VS680 UHD Smart Display SoC - EVK User Guide

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1. Introduction

The Synaptics VS680 Evaluation Kit (EVK) is an application-ready platform that enables developers to test and evaluate the VS680. The VideoSmart™ VS680 Display System-on-a-Chip (SoC) brings a potent combination of performance, and feature integration to IoT device manufacturers, enabling leading-edge multi-media products in ultra-high definition with edge computing power that can meet price points for the volume segment in worldwide markets. The EVK can also be a reference platform for subsequent development of production-ready software stacks.

The VS680 SoC integrates quad ARM core CPUs, GPU, NNA for machine learning, ISP for camera, and a secure processor to allow a wide range of secure IoT application opportunities in a cost-effective 17mm x17mm FCBGA package.

1.1. Scope

This document describes on-board hardware for intended applications, such as:

- Set-Top Box System with Voice Assistants
- Voice and AI-enabled Sound bars
- Smart display

This manual enables EVK users to evaluate specified hardware usages for operational, functional and debug purposes. This includes tasks such as availability, definition and location of IO connectors, switches and buttons, LEDs, test points, as well as pin-mux and GPIO definitions for various software controls.

Additionally, users can also follow processes that describe how to bring up this platform, run diagnostic tools, and make associated hardware connections to supporting files and software libraries. Applications covered in the document also include items addressed by hardware reconfiguration or the design of corresponding daughterboard add-ons.

This manual is applicable to VS680 EVK *V2r2* in red oil for board soldermak.

1.2. System Features

The VS680 EVK platform includes the following system components:

- On-board Main Components:
  - Synaptics VS680 VideoSmart™ Quad-Core A73 UHD smart display SoC
  - Synaptics CX9000 Class-D, 2-CH speaker AMP with 1-bit AEC data out
  - Storage: eMMC5.1 (8/16GByte)
  - DRAM: x64 2/4 GB system memory by 2pcs x32 8/16Gbit LPDDR4x
  - PMIC: two support DVFS in Vcore and Vcpu supply rails
  - IR receiver: supports remote control in NEC IR protocol
  - Push buttons: four support configurable end-user's controls such as volume up/down, menu selection, BT pair etc.

- Standard I/O Interfaces:
  - HDMI Type-A Tx interface: v2.1 with HDCP 2.2 sources up to 4K60p video and advanced audio
  - HDMI Type-A Rx interface: v2.1 with HDCP 2.2 sinks up to 4K60p video and advanced audio
  - Optical TOSHIBA TOSLINK™ Transmitter
  - Optical TOSHIBA TOSLINK™ Receiver
  - SD Card slot
  - M.2 E-key slot: supports SDIO, PCIe, UART, USB 2.0 for WiFi/BT modules
  - USB 3.0 Type-A: supports host mode at SuperSpeed
  - USB 2.0 Micro-AB: supports OTG host or peripheral mode at Hi-Speed

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- Off-board Daughter Card Interfaces:
  - MIPI DSI on 40-pin Samtec interface: supports 4-lane DSI plus I2C and GPIOs for up to 4K30p/2K60p display panel
  - MIPI CSI-2 on two 40-pin Samtec interfaces: one supports 4-lane CSI0, and one supports 2-lane CSI1, each plus I2C and GPIOs, for up to 4K60p (one camera) or 4K30p (two cameras)
  - SPI key card 1.8V version: boots and runs Diagnostics or UBoot from SPI NOR flash
  - Debug board 1.8V version: UART console over mini-USB interface, JTAG connection
  - PDM DMIC daughter card: supports two or four MEMS digital microphone modules
  - Multi-channel speaker daughter card: supports up to 8 channels of I2S audio contents to speakers
  - Sound-bar IO daughter card: Z1 to support up to 4 data lines from eARC, stereo line-in, or HDMI Rx
  - TSI daughter card: supports up to 4 streams of terrestrial, cable or satellite RF contents
  - Wired Ethernet option by on-board FE/Gbit-Ethernet transceiver or off-board low-cost Fast-Ethernet transceiver

- 12V power supply for 2.5 mm x 5.15 mm jack

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1.3. System Overview

Figure 1 shows the system block diagram and Figure 2 shows the top view of VS680 EVK Main Board.

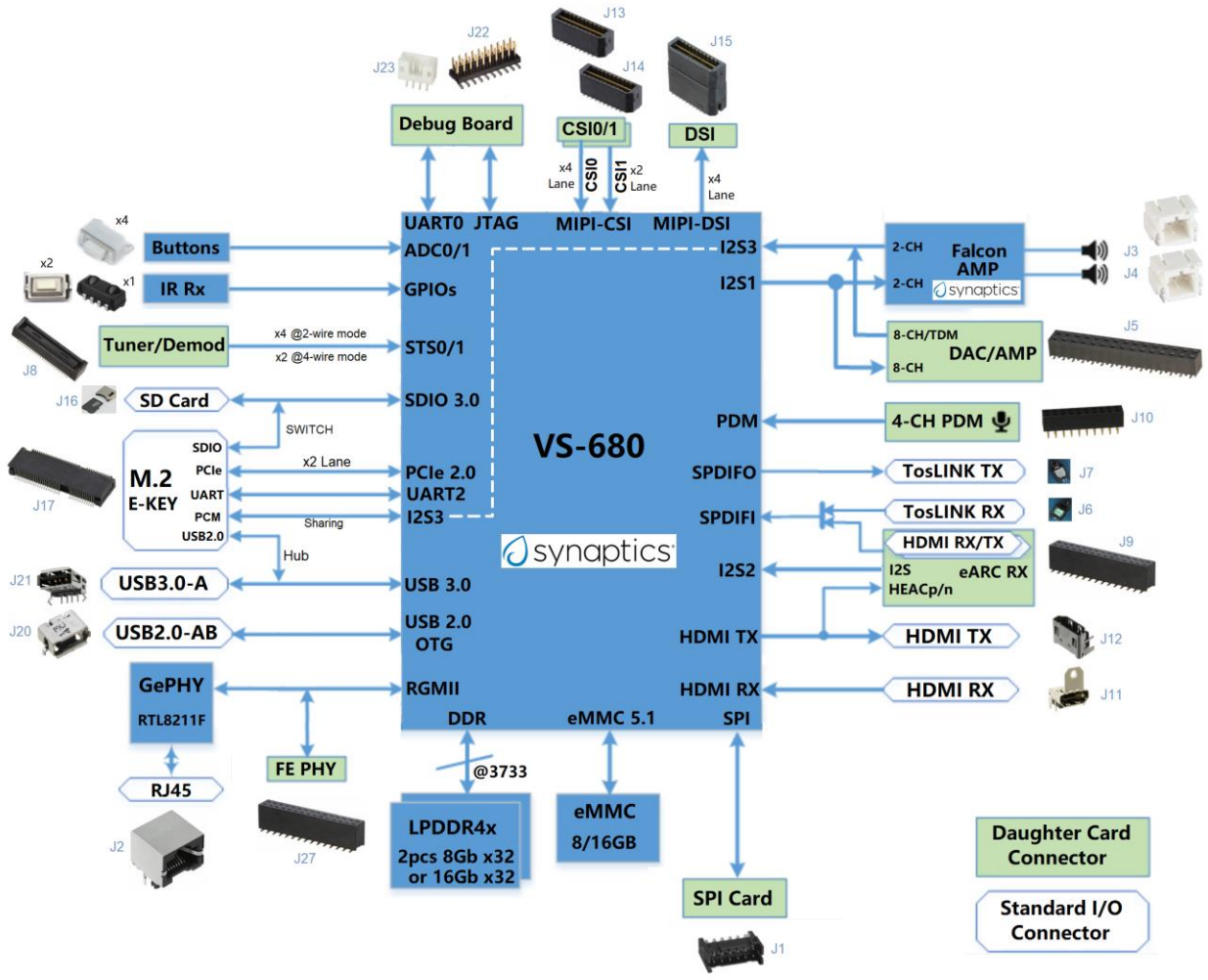


Figure 1. VS680 System Block Diagram

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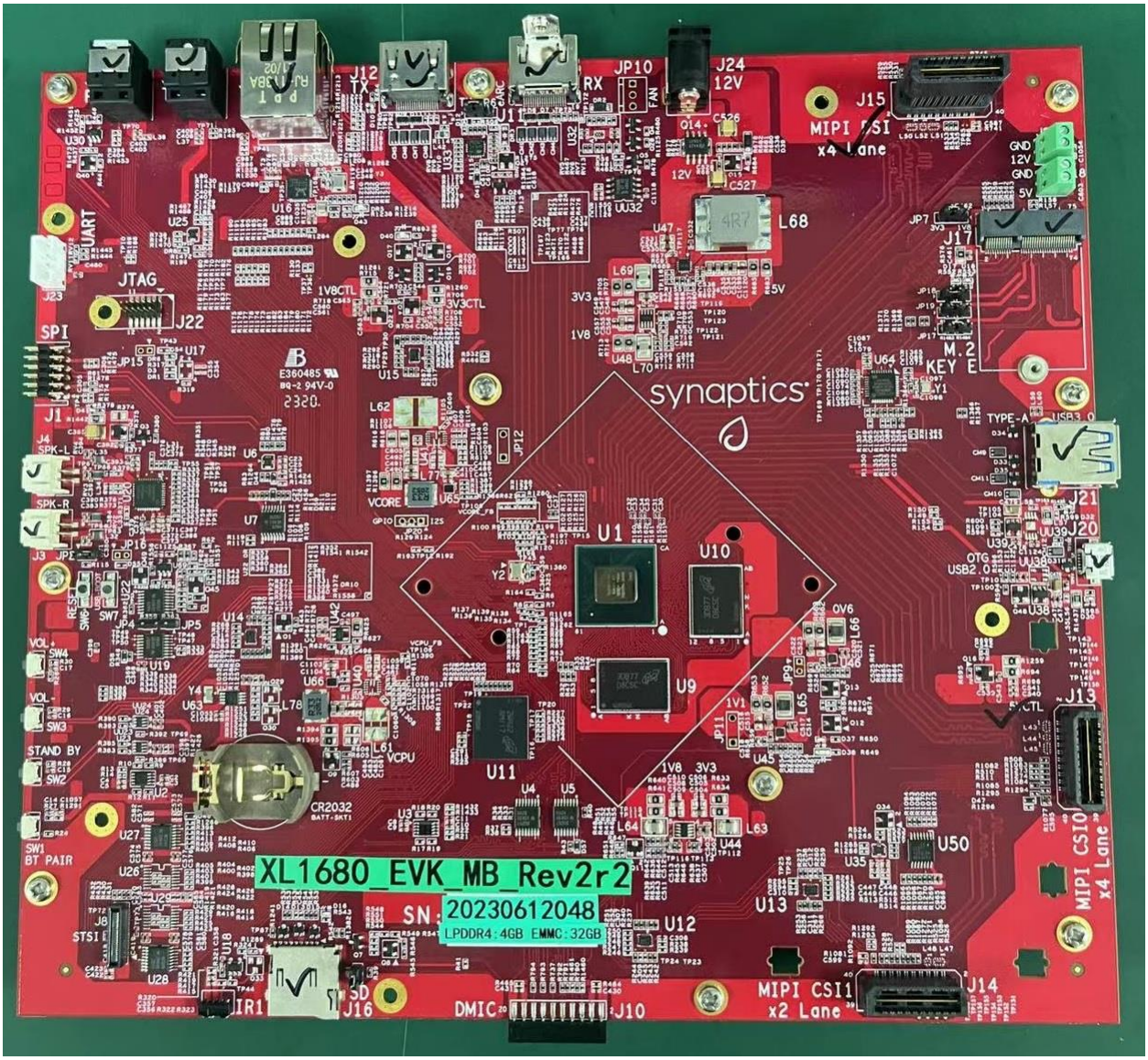


Figure 2. Top View of V680 EVK Main Board V2r2

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2. Main Board Control/Status and System I/O

This section covers LEDs, status indicators, switches, test-points, connectors and pin-strap settings on VS680 EVK Main Board.

2.1. LEDs

2.1.1. LED Locations

Figure 3 shows LED locations on VS680 Main Board.

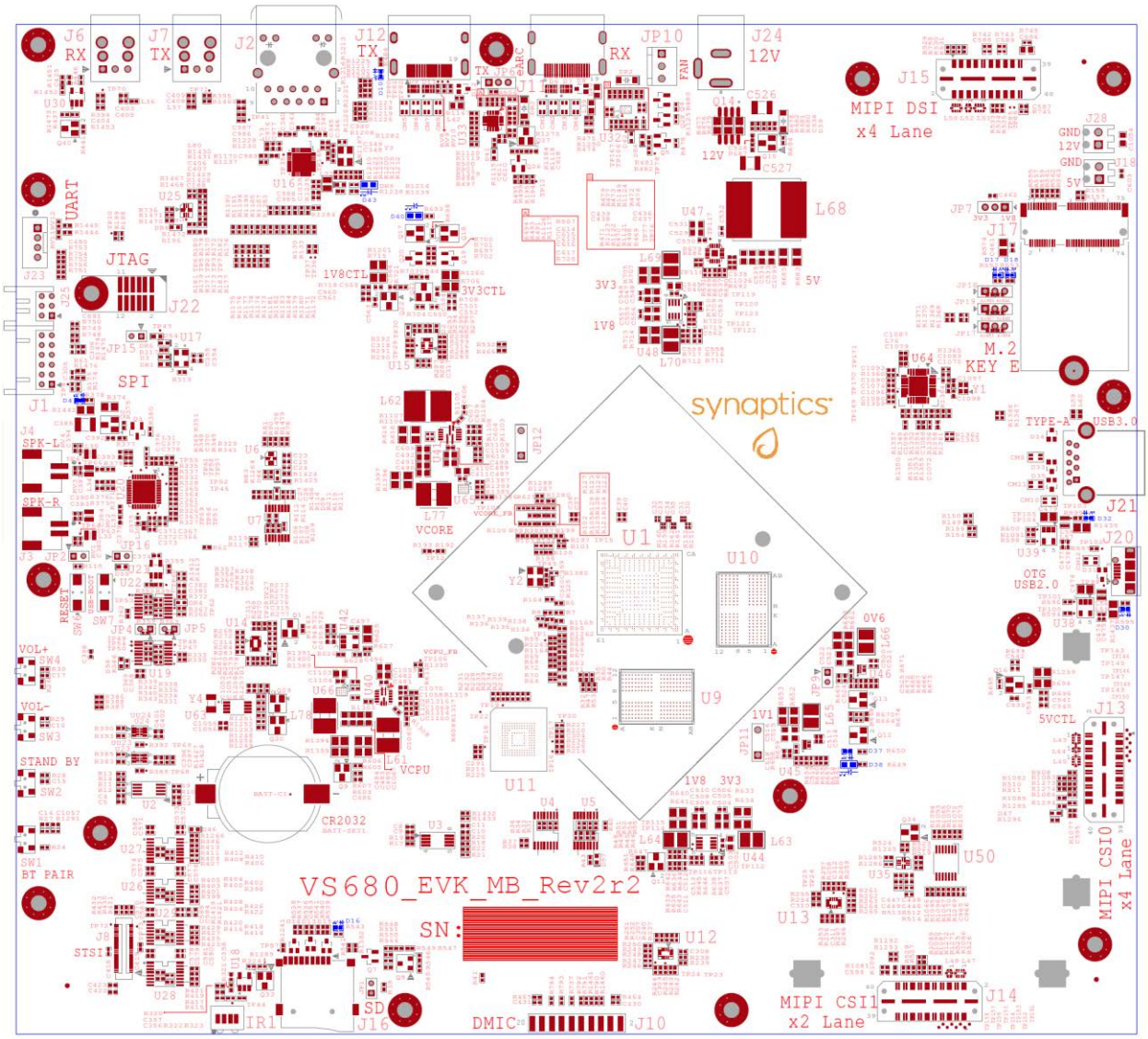


Figure 3. LED Locations on Main Board

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2.1.2. LED Definitions

Table 1 lists LED definitions.

Table 1. LED Definitions

LED	Color	Green LED Function
D4	Green	Power-up Indicator for speaker 12V power. Lit ON in normal;
D10	Green	Power-up Indicator for HDMI-TX 5V power. Lit ON in normal;
D16	Green	Power-up Indicator for SDIO Memory card slot. Lit ON in normal;
D17	Green	LED Indicator1 for M.2 device general purpose;
D18	Green	LED Indicator2 for M.2 device general purpose;
D30	Green	Power-up Indicator for USB2.0 Mircro-AB receptacle
D32	Green	Power-up Indicator for USB3.0 Type A receptacle
D37	Green	Power-up Indicator for 3.3V and LPDDR4x 1.1V power
D38	RED	Power-up Indicator for 1.8V and LPDDR4x 1.1V power
D40	RED	LED Indicator for Stand-By Status;
D43	RED	LED indicator for on-board GePHY status. Defined by PHY's internal register;

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2.2. SM (System Manager) PinStrap and Bootup Settings

Table 2. SM PinStrap and Bootup Settings

Pad Name	Strap Name	Setting Value Default*	Resistor Stuffing + stuffed - removed	Description Rpu = OnChip Pull-up Rpd = OnChip Pull-down
SM_URT0_TXD	SM_STRP[0]	—	—	SM to SOC RSTn mode select (Rpd)
		0*	-R188	0: socRstN releasing waits for SoCRstCnt but does not wait for SM_PWR_OK (mode_0 of SM_URT0_TXD, system will assert this signal when SOC core power is ready).
		1	+R188	1: socRstN releasing waits for both SoCRstCnt and SM_PWR_OK.
SM_SPI2_SDO	SM_STRP[1]	—	—	Straps for software usage (Rpd)
		0*	-R190	—
		1	+R190	—
SM_SPI2_SS0n	SM_STRP[2]	—	—	Straps for software usage (Rpd)
		0*	-R192	—
		1	+R192	—
SM_SPI2_SS1n	SM_STRP[3]	—	—	Straps for software usage (Rpd)
		0*	-R194	—
		1	+R194	—
SM_TEST_EN	SM_TEST_EN	—	—	SM TEST Enable (Rpd)
		0*	-R184	0: Enable ARM ICE JTAG connections (CoreSight)
		1	+R184	1: Enable SCAN or BSCAN tests
SM_JTAG_SEL	SM_JTAG_SEL	—	—	SM JTAG Port Selection (Rpd)
		0*	-R186	0: ARM ICE JTAG connections
		1	+R186	1: Reserved for factory use
SM_POR_EN	SM_POR_EN	—	—	Power-on reset (POR) bypass (Rpu)
		0	+R3	0: Bypass on-chip POR generator
		1*	-R3	1: Enable on-chip POR generator

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2.3. SoC (System on Chip) PinStrap and Bootup Settings

Table 3. SoC PinStrap and Bootup Settings

Pad Name	Strap Name	Setting Value Default*	Resistor Stuffing + stuffed - removed	Description Rpu = OnChip Pull-up Rpd = OnChip Pull-down
RGMII_TXD[2]	cpuRstByps	—	—	CPU reset bypass strap (Rpd)
		0*	-R178	0: Enable reset logic inside CPU partition
		1	+R178	1: Bypass reset logic inside CPU partition
RGMII_TXD[3]	pllPwrDown	—	—	SYS/MEM/CPU PLL Power Down; Note: pllPwrDown should be set to 1 only when pllByps is also set to 1. (Rpd)
		0*	-R180	0: Power up
		1	+R180	1: Power down
RGMII_TXCTL	pllByps	—	—	SYS/MEM/CPU PLL bypass indicator
		0*	-R182	0: No bypass
		1	+R182	1: All PLL bypassed
SPI1_SDO	software_strap[0] (USB_BOOTn)	—	—	ROM code uses this strap to determine if booting from USB or not (Rpu)
		0	—	0: Boot from USB when SW7 is pressed while power-up or system reset de-assertion
		1*	—	1: Boot from the device select by boot_src
SPI1_SS0n	software_strap[1]	—	—	Straps for software usage (Rpd)
		0*	-R174	—
		1	+R174	—
RGMII_TXD[0]	software_strap[2]	—	—	Straps for software usage (Rpd)
		0*	-R172	—
		1	+R172	—
RGMII_TXD[1]	software_strap[3]	—	—	Straps for software usage (Rpd)
		0*	-R170	—
		1	+R170	—
SPDIFO	boot_src[1]	—	—	CPU Boot Source bit [1] (Rpu) See boot_src [1:0]
		0	—	SPI Key JP10=2-3.
		1*	—	SPI Key JP10=1-2, or no SPI Key
I2S2_MCLK	boot_src[0]	—	—	CPU Boot Source bit [0] (Rpd) See boot_src [1:0]
		0*	—	SPI Key JP11=2-3, or no SPI Key
		1	—	SPI Key JP11=1-2

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{ SPDIFO, I2S2_MCLK }	boot_src [1:0]	—	—	SPI Key JP10:JP11=[:]
		0, 0	—	ROM boot from SPI. [2-3:2-3]
		0, 1	—	Reserved [2-3:1-2]
		1, 0*	—	ROM boot from EMMC [1-2:2-3], or no SPI Key
		1, 1	—	Reserved for factory use only [1-2:1-2]
RGMII_TXC	Legacy_boot	—	—	Strap to reduce reset wait time
		0	-R176	0: 2 ms
		1	+R176	1: 20 ms

2.4. Hardware Manual Button Settings

Table 4. Hardware Manual Button Settings Definitions

Switch Block	Type	Switch #	Setting	Function
SW1	Momentary Pushbutton	N/A	Push	BT Pairing Request Key asserted
			Release	Key de-asserted
SW2	Momentary Pushbutton	N/A	Push	Stand-By Request Key asserted
			Release	Key de-asserted
SW3	Momentary Pushbutton	N/A	Push	VOL- Key asserted
			Release	Key de-asserted
SW4	Momentary Pushbutton	N/A	Push	VOL+ Key asserted
			Release	Key de-asserted
SW6	Momentary Pushbutton	N/A	Push	VS680 Reset Key asserted
			Release	Key de-asserted
SW7	Momentary Pushbutton	N/A	Push	USB boot Key asserted. Need combo SW6.
			Release	Key de-asserted. Need combo SW6.

To enter USB-Boot mode, follow these steps (prior to these steps, make sure the USB driver is installed successfully on PC host side):

1. Push SW6 to assert system reset to VS680;
2. Keep pushing SW6 and push SW7 at the same time for 1-2 second;
3. Release SW6 while holding SW7 so VS680 boots in USB-Boot mode;
4. Check and wait for the console print….
5. Once the console print is returned and the USB-Boot is entered successfully, release SW7.

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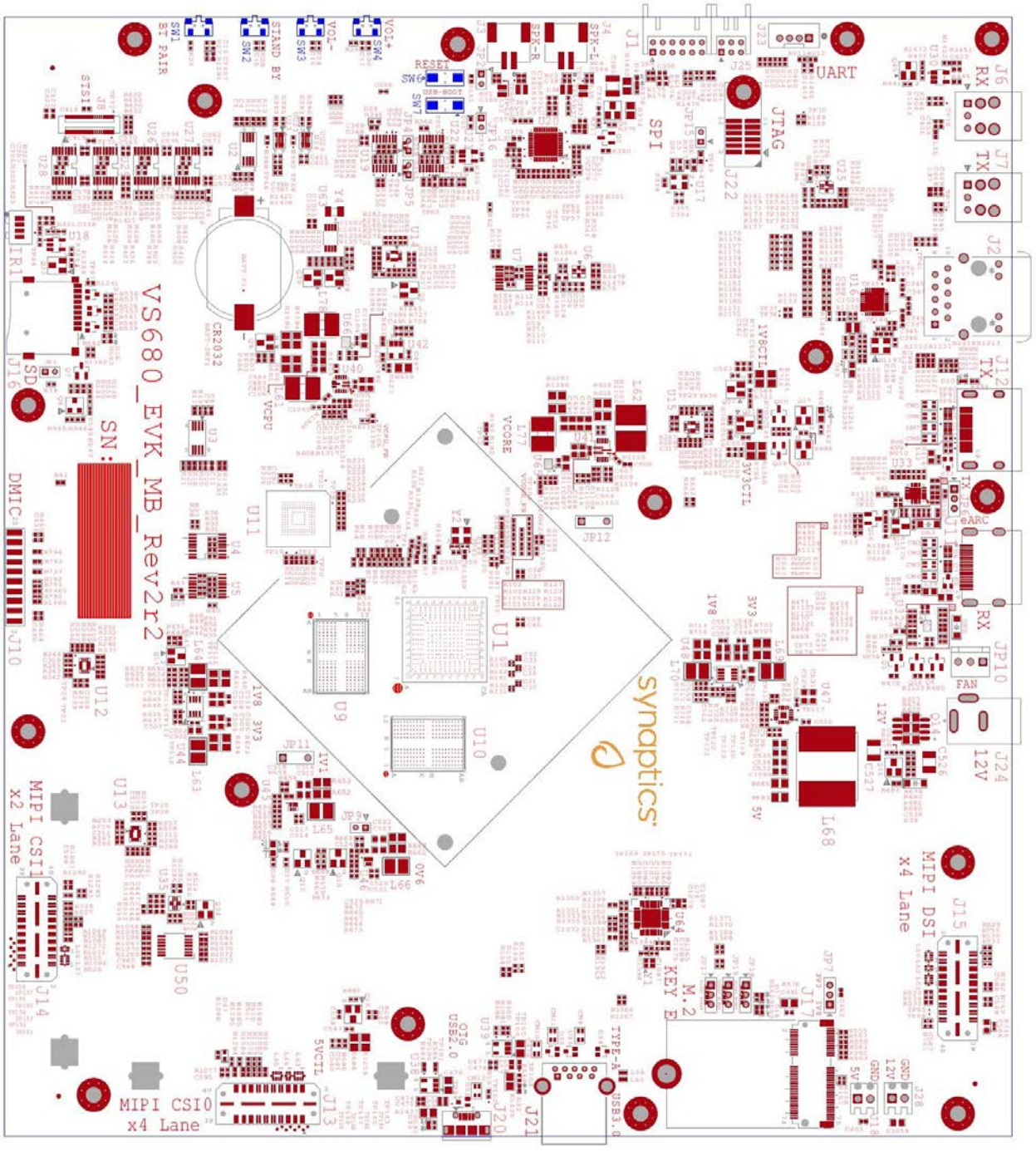


Figure 4. Locations of Manual Buttons on Top Side

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2.5. Hardware Jumper Settings

Table 5. Hardware Jumper Settings Definitions

Ref Des	Type	Pin Connection	Description
JP1	2x1 2mm header	1-2	SDIO path to Memory Card or M.2 Module:
			• Open: SDIO to Memory Card at J16
			• Short: SDIO to M.2 Module at J17
JP2	2x1 2mm header	1-2	I2S2 data bit & SPDIF IN selection:
			• Open: 4-bit without SPDIF IN (Default)
			• Short: 2-bit & SPDIF IN available
JP4	2x1 2mm header	1-2	I2S BCLK external loop-back from I2S1 to I2S3:
			• Open: loop-back disabled (Default)
			• Short: loop-back enabled
JP5	2x1 2mm header	1-2	I2S LRCLK external loop-back from I2S1 to I2S3
			• Open: loop-back disabled (Default)
			• Short: loop-back enabled
JP15	2x1 2mm header	1-2	System reset from external host for automatic test extension (NOT stuffed)
			• Pin 1 for reset from external host
			• Pin 2 for GND from external host
JP16	2x1 2mm header	1-2	USB_BOOTn control from external host for automatic test extension
			• Pin 1 for USB_BOOTn control from external host
			• Pin 2 for GND from external host
JP6	3x1 2mm header	—	HDMI_HPD IN source selection
		1-2	• From HDMI Source connector J12 (Default)
		2-3	• From eARC GPIO via Sound-bar IO Card at J9
JP7	3x1 2mm header	—	VIO voltage selection for M.2 device at J17
		1-2	• 1.8V
		2-3	• 3.3V
JP17	3x1 2mm header	—	M2-KEYE_HOST_WAKEn to M.2 Device selection at J17
		1-2	• AMPAK AP12275_M2P (BroadCom 2x2 PCIe+UART)
		2-3	• AzerWave CM276MA/CM358SM or Eardatek 8822CSS3AA
JP18	3x1 2mm header	—	M.2-Pin38 selection for M.2 device at J17
		1-2	• BT_DEV_WAKE by AMPAK
		2-3	• VIO by AzerWave or Eardatek
JP19	3x1 2mm header	—	M.2-Pin40 selection for M.2 device at J17
		1-2	• WL_HOST_WAKE by AMPAK
		2-3	• VIO_SD by AzerWave
JP9	2x1 2mm header	1-2	PMIC Vout for VDDQ of LPDDR4x (NOT stuffed, fixed 0.6V in default)
			• Open: 1.1V;
			• Short: 0.6V (Default)

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Table 6. M.2 Module choice with jumper combo settings

M.2 Module P/N	Jumper Positions			
	JP7	JP17	JP18	JP19
AP12275_M2P	2-3	1-2	1-2	1-2
AW-CM276MA / CM358SM	1-2	2-3	2-3	2-3
AW-CM358SM	1-2	2-3	2-3	2-3

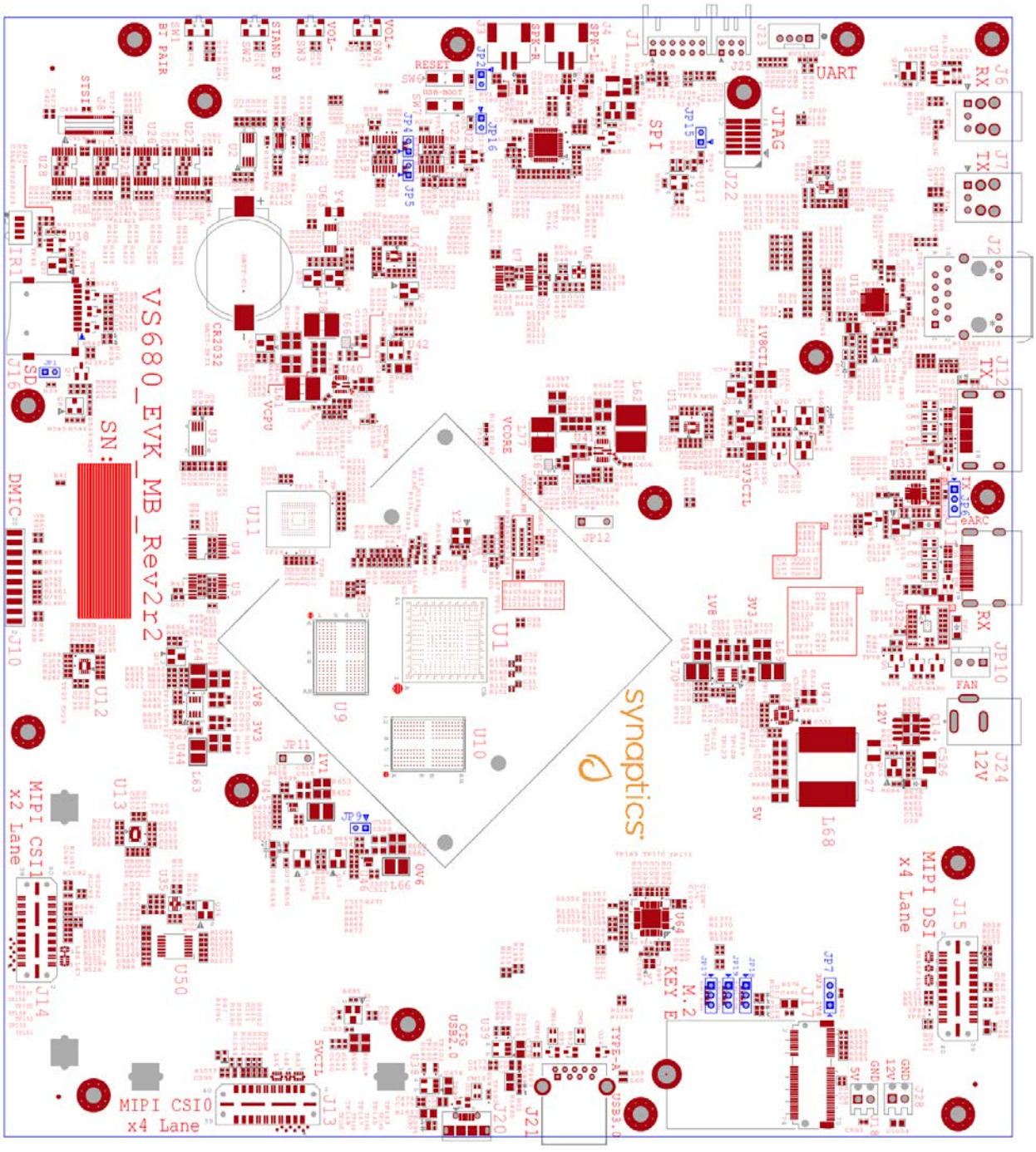


Figure 5. Locations of Jumper Settings on Top Side

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2.6. Main Board Test Points

2.6.1. Locations of Main Board Test Points on Top Side

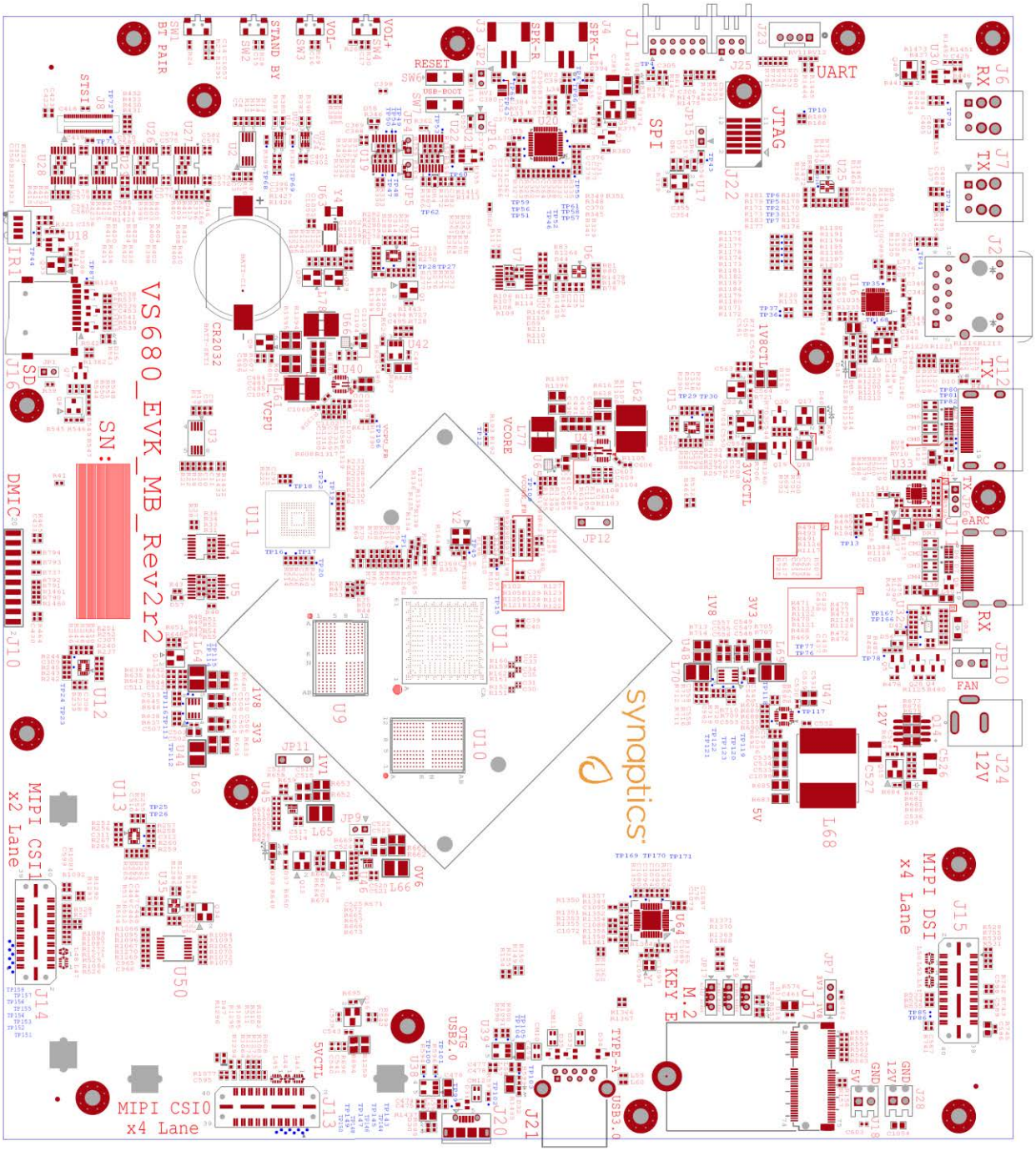


Figure 6. Locations of Main Board Test Points on Top Side

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2.6.2. Locations of Main Board Test Points on Bottom Side



Figure 7. Locations of Main Board Test Points on Bottom Side

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2.6.3. Main Board Test Point Definitions

Table 7. Main Board Test Point Definitions

Ref Des	Form	Signal	Comments
TP1	smd pad	VS680.VDDIO1P8.LN.SPI1_SDO&&STRP[USB_BOOTn]@PUBoot	For STRP[USB_BOOTn]
TP2	smd pad	VS680.VDDIO1P8.LN.RGMII_TXD1&&STRP[SS3]@PDBoot	For STRP[SS3]
TP3	smd pad	VS680.VDDIO1P8.LN.RGMII_TXD0&&STRP[SS2]@PDBoot	For STRP[SS2]
TP4	smd pad	VS680.VDDIO1P8.SPI1_SS0n&&STRP[SS1]@PDBoot	For STRP[SS1]
TP5	smd pad	VS680.VDDIO1P8.LN.RGMII_TXD2&&STRP[cpuRstByps]@PDBoot	For STRP[cpuRstByps]
TP7	smd pad	VS680.VDDIO1P8.LN.RGMII_TXD3&&STRP[pllPwrDown]@PDBoot	For STRP[pllPwrDown]
TP8	smd pad	VS680.VDDIO1P8.LN.RGMII_TXCTL&&STRP[pllByps]@PDBoot	For STRP[pllByps]
TP9	smd pad	VS680.SM_VDDIO1P8.TEST_EN@PD	For SM-TEST_EN
TP10	smd pad	VS680.SM_VDDIO1P8.SM_URT0_TXD&&STRP[SM_SS0]@PDBoot	For STRP[SM_SS0]
TP11	smd pad	VS680.SM_VDDIO1P8.SM_SPI2_SDO.DMX.SM_URT2_RTSn&&STRP[SM_SS1]@PDBoot	For STRP[SM_SS1]
TP12	smd pad	VS680.SM_VDDIO1P8.SM_SPI2_SS0n.DMX.SM_GPO17&&STRP[SM_SS2]@PDBoot	For STRP[SM_SS2]
TP13	smd pad	VS680.SM_VDDIO1P8.SM_SPI2_SS1n.DMX.SM_GPO16&&STRP[SM_SS3]@PDBoot	For STRP[SM_SS3]
TP14	smd pad	VS680.VDDIO1P8.LN.SPDIFO&&STRP[boot_src1]@PUBoot	For STRP[boot_src1]
TP15	smd pad	VS680.VDDIO1P8.I2S2_MCLK&&STRP[boot_src0]@PDBoot	For STRP[boot_src0]
TP16	smd pad	VS680.EMMC_VDDIO18.LN.eMMC_CMD	For eMMC_CMD
TP17	smd pad	VS680.EMMC_VDDIO18.LN.eMMC_CLK	For eMMC_CLK
TP18	smd pad	VS680.EMMC_VDDIO18.eMMC_RSTn	For eMMC_RSTn
TP19	smd pad	VS680.EMMC_VDDIO18.LN.eMMC_DATA0	For eMMC_DATA0
TP20	smd pad	VS680.EMMC_VDDIO18.eMMC_STRB	For eMMC_STRB
TP21	smd pad	PWR_eMMC_VDDi	For PWR_eMMC_VDDi
TP22	smd pad	GND	Ground
TP23	smd pad	SM_EXPANDER0 Reset	For SM_EXPANDER0 Reset
TP24	smd pad	SM_EXPANDER0.ADDR	For SM_EXPANDER0.ADDR
TP25	smd pad	SM_EXPANDER1.RSTn	For SM_EXPANDER1.RSTn
TP26	smd pad	SM_EXPANDER1.ADDR	For SM_EXPANDER1.ADDR
TP27	smd pad	SOC_EXPANDER2.RSTn	For SOC_EXPANDER2.RSTn
TP28	smd pad	SOC_EXPANDER2.ADDR	For SOC_EXPANDER2.ADDR
TP29	smd pad	SOC_EXPANDER3.RSTn	For SOC_EXPANDER3.RSTn

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Ref Des	Form	Signal	Comments
TP30	smd pad	SOC_EXPANDER3.ADDR	For SOC_EXPANDER3.ADDR
TP35	smd pad	GePHY_RSTn	For GePHY_RSTn
TP36	smd pad	VS680.VDDIO1P8.LN.RGMII_MDIO	For RGMII_MDIO
TP37	smd pad	VS680.VDDIO1P8.LN.RGMII_MDC	RGMII_MDC
TP41	smd pad	PWR_RJ45_TRFM	For PWR_RJ45_TRFM
TP43	smd pad	VS680.SM_VDDIO1P8.SM_RSTIn@PU	For SM_RSTIn
TP44	smd pad	EXT_IR_OUT	For IR_OUT
TP45	smd pad	VS680.SMOSC_VDDIO1P8.SM_CLKO	For SM_CLKO
TP46	smd pad	SPEAKER_ENABLE	For SPEAKER_ENABLE
TP47	smd pad	VS680.VDDIO1P8.DMX.I2S1_DO1	For I2S1_DO1
TP48	smd pad	VS680.VDDIO1P8.LN.I2S1_DO0	For I2S1_DO0
TP49	smd pad	VS680.VDDIO1P8.LN. I2S1_LRCK	For I2S1_LRCK
TP50	smd pad	VS680.VDDIO1P8.LN.I2S1_LRCK	For I2S1_LRCK
TP51	smd pad	PWR_SPK_VCORE	For PWR_SPK_VCORE
TP52	smd pad	SPEAKER_I2S-SD-IN	For SPEAKER_I2S-SD-IN
TP53	smd pad	CONN-SPK_CARD-DETn@3V3	For CONN-SPK_CARD-DETn
TP54	smd pad	SPEAKER_I2S-BCLK	For SPEAKER_I2S-BCLK
TP55	smd pad	SPEAKER_I2S-ADCDAT	For SPEAKER_I2S-ADCDAT
TP56	smd pad	PWR_SPK_AVDD1P8	For PWR_SPK_AVDD1P8
TP57	smd pad	SPEAKER_I2S-MCLK	For SPEAKER_I2S-MCLK
TP58	smd pad	SPEAKER_I2S-LRCK	For SPEAKER_I2S-LRCK
TP59	smd pad	SPK_BIAS	For SPK_BIAS
TP60	smd pad	VS680.VDDIO1P8.DMX.I2S3_DI	For I2S3_DI
TP61	smd pad	PWR_SPK_AVDD5	For PWR_SPK_AVDD5
TP62	smd pad	VS680.VDDIO1P8.I2S3_DO.DMX.GPIO1	For SPK_IRQ IN
TP63	smd pad	CONN_SPK-Rp	For HDMI_CEC close Connector
TP64	smd pad	CONN_SPK-Rn	For HDMI_ARC close Connector
TP65	smd pad	PWR_SPK_PVDD	For PWR_SPK_PVDD
TP66	smd pad	CONN_SPK-Ln	For SPK-Ln to CONN
TP67	smd pad	CONN_SPK-Lp	For SPK-Lp to CONN
TP68	smd pad	VS680.VDDIO1P8.TW0_SCL	For TW0_SCL
TP69	smd pad	VS680.VDDIO1P8. TW0_SDA	For TW0_SDA

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Ref Des	Form	Signal	Comments
TP70	smd pad	SPDIFO_CONN	For SPDIFO to CONN
TP71	smd pad	SPDIFI_CONN	For SPDIFI from CONN
TP72	smd pad	RVSD at J8.50	For extension
TP73	smd pad	RVSD at J8.49	For extension
TP74	smd pad	MCLK at J9.2 for I2S2 IN	For MCLK at J9.2
TP75	smd pad	CONN_HDMI-RX_CEC	For CONN_HDMI-RX_CEC
TP76	smd pad	VS680.SM_VDDIO1P8.SM_TW2_SCL.DMX.HDMI-RX_EDID_SCL	For HDMI-RX_EDID_SCL
TP77	smd pad	VS680.SM_VDDIO1P8.SM_TW2_SDA.DMX.HDMI-RX_EDID_SDA	For HDMI-RX_EDID_SDA
TP78	smd pad	VS680.SM_VDDIO1P8.SM_SPI2_SS0n.DMX.SM_GPO17&& STRP[SM_SS2]@PDBoot	For STRP[SM_SS2]
TP79	smd pad	PWR_HDMITX_5V	For PWR_HDMITX_5V
TP80	smd pad	CONN_HDMI-TX_CEC	For CONN_HDMI-TX_CEC
TP81	smd pad	CONN_HDMI-TX_SCL	For CONN_HDMI-TX_SCL
TP82	smd pad	CONN_HDMI-TX_SDA	For CONN_HDMI-TX_SDA
TP85	smd pad	RVSD at J15.34	For extension
TP86	smd pad	RVSD at J15.36	For extension
TP87	smd pad	CONN_SD0_CDn	For CONN_SD0_CDn
TP88	smd pad	PWR_SD0_3V3OUT	For PWR_SD0_3V3OUT
TP89	smd pad	VS680.VDDIO1P8.DMX.I2S3_BCLK	For I2S3_BCLK
TP90	smd pad	VS680.VDDIO1P8.DMX.I2S3_LRCK	For I2S3_LRCK
TP91	smd pad	VS680.VDDIO1P8.DMX.I2S3_DI	For I2S3_DI
TP92	smd pad	VS680.VDDIO1P8.DMX.I2S3_DO	For I2S3_DO
TP93	smd pad	M2-KEYE_UART-RXD	For M2-KEYE_UART-RXD
TP94	smd pad	M2-KEYE_UART-TXD	For M2-KEYE_UART-TXD
TP95	smd pad	M2-KEYE_UART-CTSn	For M2-KEYE_UART-CTSn
TP96	smd pad	M2-KEYE_UART-RTSn	For M2-KEYE_UART-RTSn
TP97	smd pad	M2-KEYE_SLP_CLK	For M2-KEYE_SLP_CLK
TP98	smd pad	RVSD at J17.62	For extension
TP99	smd pad	PWR_OTG_VBUS	For PWR_OTG_VBUS
TP100	smd pad	EXPANDER.V3P3-CTRL.SoC-TW0.GPIO2_3	For USB2- CONN _PWR_ON
TP101	smd pad	EXPANDER.V1P8-CTRL.SoC-TW0.GPIO3_0	For USB2- CONN _OVn
TP102	smd pad	CONN_USB0_ID	For CONN_USB0_ID
TP103	smd pad	PWR_USB3_VBUS	For PWR_USB3_VBUS

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Ref Des	Form	Signal	Comments
TP104	smd pad	EXPANDER.V3P3-CTRL.SoC-TWO.GPIO2_2	For USB3-CONN_PWR_ON
TP105	smd pad	EXPANDER.V3P3-CTRL.SoC-TWO.GPIO2_1	For USB3-CONN_OVn
TP106	smd pad	VS680.VDD_CPU.FDBK	For VDD_CPU.FDBK
TP109	smd pad	VS680.VDD_CORE.FDBK	For VDD_CORE.FDBK
TP112	smd pad	PWR_5V	Vin For PMIC SY8832-2
TP113	smd pad	SY8832-2_Vfb1	For SY8832-2_Vfb1
TP114	smd pad	SY8832-2_EN1	For SY8832-2_EN1
TP115	smd pad	SY8832-2_EN2	For SY8832-2_EN2
TP116	smd pad	SY8832-2_Vfb2	For SY8832-2_Vfb2
TP117	smd pad	PWR_12V	Vin For 12V to 5V PMIC SY8286A
TP118	smd pad	SY8286A_FB	Vfb For 12V to 5V PMIC SY8286A
TP119	smd pad	PWR_5V	Vin For PMIC SY8832-1
TP120	smd pad	SY8832-1_Vfb1	For SY8832-1_Vfb1
TP121	smd pad	SY8832-1_EN1	For SY8832-1_EN1
TP122	smd pad	SY8832-1_EN2	For SY8832-1_EN2
TP123	smd pad	SY8832-1_Vfb2	For SY8832-1_Vfb2
TP124	smd pad	VS680.MIPI_DSI_AVDD1P8.MIPI_DSI_ATB	For MIPI_DSI_ATB
TP125	smd pad	VS680.MIPI_CSI0_AVDD1P8.MIPI_CSI0_ATB	For MIPI_CSI0_ATB
TP143	smd pad	RSVD for J13.1	For extension
TP144	smd pad	RSVD for J13.3	For extension
TP145	smd pad	RSVD for J13.5	For extension
TP146	smd pad	RSVD for J13.7	For extension
TP147	smd pad	RSVD for J13.9	For extension
TP148	smd pad	RSVD for J13.11	For extension
TP149	smd pad	RSVD for J13.13	For extension
TP150	smd pad	RSVD for J13.15	For extension
TP151	smd pad	RSVD for J14.1	For extension
TP152	smd pad	RSVD for J14.3	For extension
TP153	smd pad	RSVD for J14.5	For extension
TP154	smd pad	RSVD for J14.7	For extension
TP155	smd pad	RSVD for J14.9	For extension
TP156	smd pad	RSVD for J14.11	For extension

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Ref Des	Form	Signal	Comments
TP157	smd pad	RSVD for J14.13	For extension
TP158	smd pad	RSVD for J14.15	For extension
TP161	smd pad	RSVD for J17.66	For extension
TP162	smd pad	RSVD for J17.68	For extension
TP163	smd pad	RSVD for J17.70	For extension
TP166	smd pad	CONN_HDMI-RX_SCL	For CONN_HDMI-RX_SCL
TP167	smd pad	CONN_HDMI-RX_SDA	For CONN_HDMI-RX_SDA
TP168	smd pad	RSVD for U16.35	For GePHY CLKOUT
TP169	smd pad	USB-HUB_PWR_EN3	For USB-HUB_PWR_EN3
TP170	smd pad	USB-HUB_PWR_EN2	For USB-HUB_PWR_EN2
TP171	smd pad	USB-HUB_PWR_EN1	For USB-HUB_PWR_EN1

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2.7. Main Board Connectors

2.7.1. Locations of Main Board Connectors on Top Side

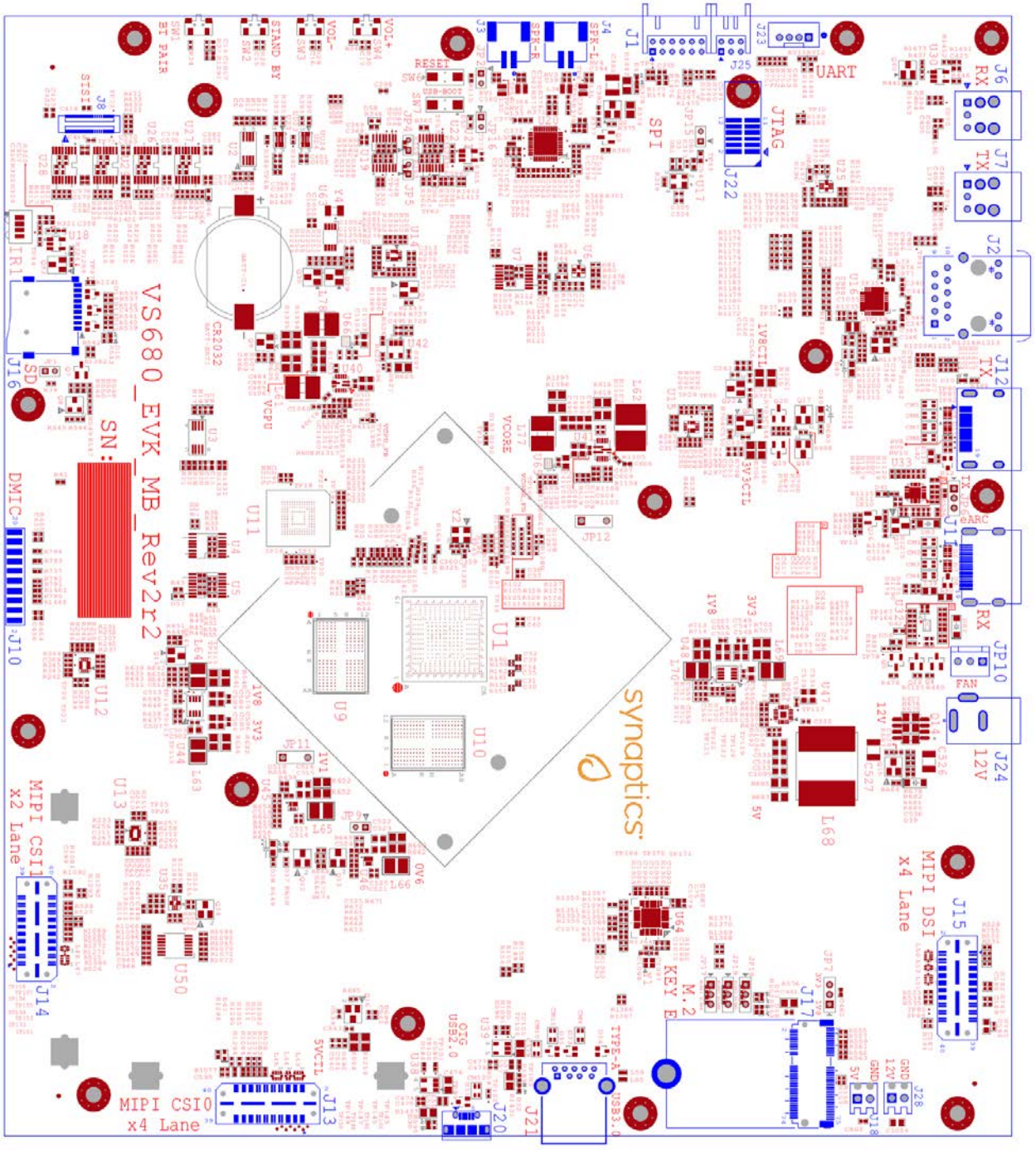


Figure 8. Locations of Main Board Connectors on Top Side

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2.7.2. Locations of Main Board Connectors on Bottom Side

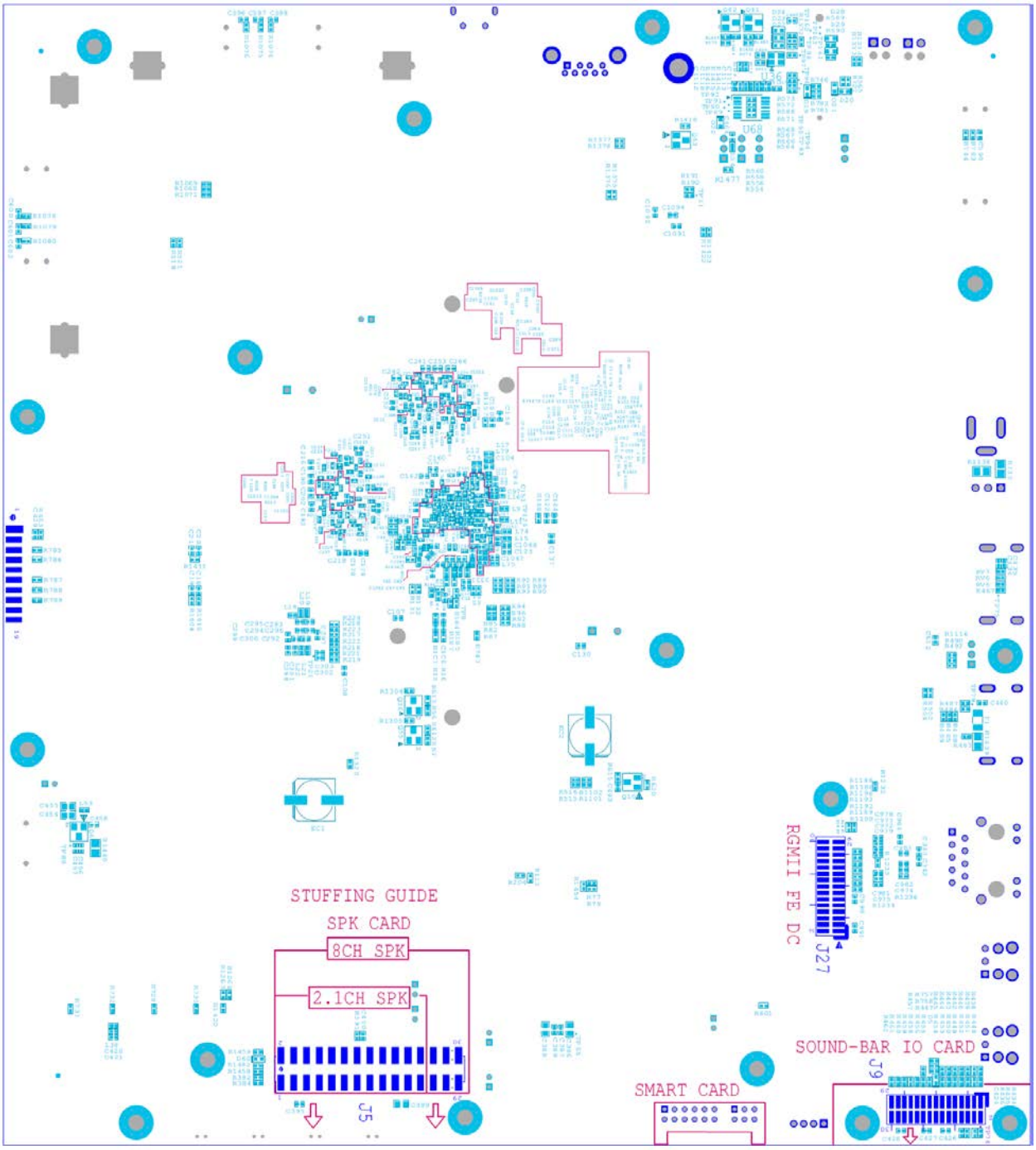


Figure 9. Locations of Main Board Connectors on Bottom Side

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2.7.3. Main Board Connector Definitions

Table 8. Main Board Connector Definitions

Main Ref Des	Connecting Boards/Devices (Ref Des if any)	Functions	Remarks
J1	SPI Flash D/C	SPI Flash	New 6x2 2.0 mm pitch card for either diagnostic or U-boot image storage. Note card's solder-mask oil in red;
J2	RJ45 cable	GigaEthernet	For Wired Ethernet connection
J3	Speaker	I2S OUT	For off-board speaker connection
J4	Speaker	I2S OUT	For off-board speaker connection
J5	Multi-CH SPK D/C	I2S to Speaker	Multi-Channel Speaker extension to 2.1/7.1-CH
J6	TosLink TX Host	TosLink RX	TosLink Optical Receiver
J7	TosLink RX device	TosLink TX	TosLink Optical Transmitter
J8	Tuner/Demod D/C	STS IN	For DVB-TC card extension
J9	Sound-Bar IO D/C	I2S IN	For 4-bit I2S data source by off-board eARC or 2-bit by ADC
J10	DMIC D/C	PDM	10 x 2 2.0 mm pitch DMIC MEMs Module card, x2 or x4 pcs
J11	HDMI Source	HDMI RX	For off-board HDMI Source host connection
J12	HDMI Sink	HDMI TX	For off-board HDMI Sink device connection
J13	MIPI-CSI0 adaptor	MIPI-CSI	For MIPI-CSI x4 lane extension, like camera
J14	MIPI-CSI1 adaptor	MIPI-CSI	For MIPI-CSI x2 lane extension, like camera
J15	MIPI-DSI adaptor	MIPI-DSI	For MIPI-DSI x4 lane extension, like panel
J16	MicroSD Card	SDIO	For mirco SD type of memory card extension
J17	M2 2230 D/C	SDIO or PCIe	1pcs 1x1/2x2 WiFi/Bluetooth card via SDIO or 1pcs PCIe with form factor at 2230.
	Extender M.2 Card	SDIO and PCIe	1pcs 1x1/2x2 WiFi/Bluetooth card via SDIO and 1 pcs PCIe device via M.2 or Mini type of receptacle;
J18	+5V power source	Power jack	Provision to DSI adaptor for bigger current +5V power source
J28	+12V power source	Power jack	Provision to DSI adaptor for bigger current +12V power source
J20	USB Device or Host	USB OTG	For USB2.0 extension, in either Host or Device mode
J21	USB Device	USB 3.0	For USB3.0 extension in Device mode only
J22	Debug Board	JTAG	XDB debugger for debugging
J23	Debug Board	UART	UART terminal Only for Console
J24	+12V AC-DC supply	Power Supply	Power for EVK rated at 12V/5A
J27	Fast Ethernet D/C	RGMII	For Fast Speed Ethernet Extension over RGMII
JP10	FAN	Heat Dissipation	For heat-sink

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3. Daughter Cards

A set of daughter cards supplements the EVK with a variety of I/O peripheral functionalities. Perspective devices offered by different manufacturers for each of such I/Os may be implemented using respective daughter card.

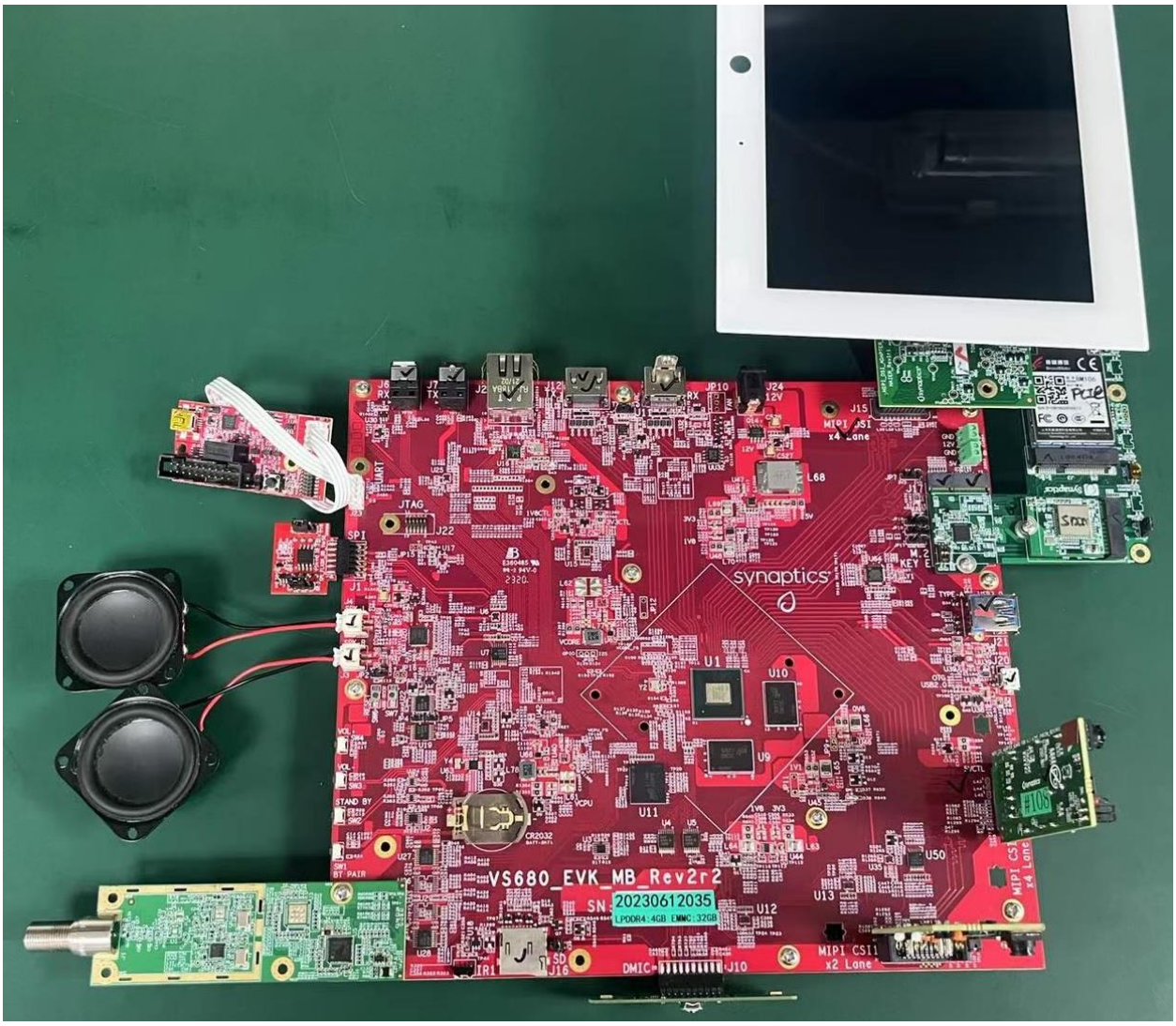


Figure 10. Daughter Cards around the VS680 EVK System

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Debug Board Rev.5

Debug Board Rev5 (not older revisions) allows users communicating with VS680 over UART on a PC host. It is based on the Silicon Labs CP2102 USB to UART bridge designed on the debug board. A virtual COM port driver is required, and can be downloaded from the following link and installed in the PC host:

https://www.silabs.com/products/development-tools/software/usb-to-uart-bridge-vcp-drivers

Only if necessary, the debug board also allows users communicating with VS680 over JTAG through an XDB Debugger on a PC host. While connecting EVK and Debug Board with a 20-pin flat cable, align pin-1 of the 2x10 cable socket at EVK side with pin-1 of J22, a 2x6 header, on EVK.

EVK UART and the PC host USB are digitally isolated, with no direct conductive path, eliminating ground loop and back-drive issues when either is powered down.

Figure 11 shows debug board connectivity facilitating UART and JTAG communications.

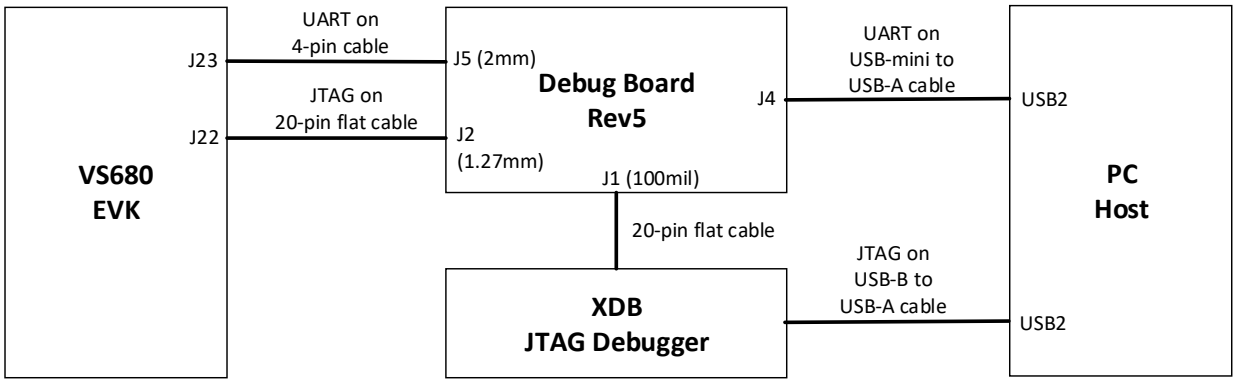


Figure 11. Debug Board Connectivity for UART and JTAG

Figure 12 shows the debug board headers.

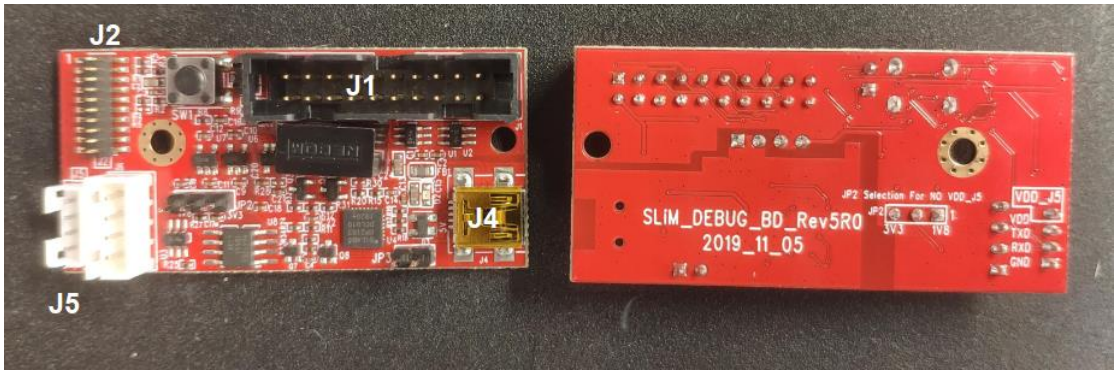


Figure 12. Debug Board Headers (top and bottom views)

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3.1. SPI Card Rev.5

VS680 may boot from an off-board SPI NOR flash using an SPI Card Rev5 (not older revisions) connected on the VS680 EVK at J1. The NOR flash may be programmed with diagnostics or U-Boot binary depending on the requirements.

VS680 can automatically detect SPI card and boots from it as long as the card is plugged on J1 of EVK, with the default jumper setting – JP10/JP11 at pin2-3/pin2-3. Although it is possible to boot from other NAND or eMMC storage devices with the card plugged in, as shown below, it is recommended to simply remove the card when the SPI flash is not intended to be the boot source.

Table 9. SPI Card boot source jumper settings

Jumper Settings		
JP10	**JP11**	**Config**
1–2	1–2	SPI_CLR
2–3	*1–2*	*NAND (Not Available)*
1–2	2–3	eMMC
2–3	2–3	SPI_Sec

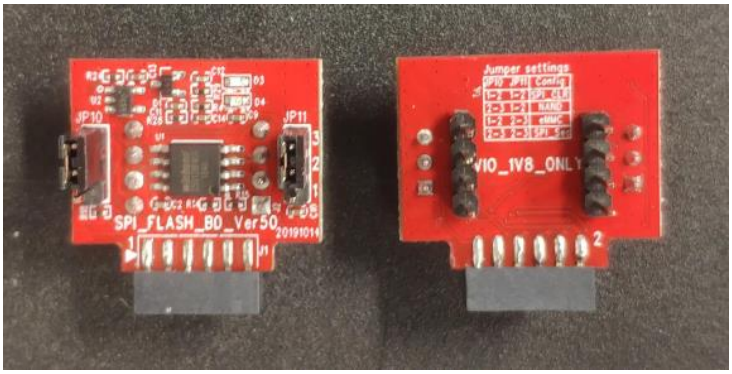


Figure 13. SPI Card (top and bottom views)

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3.2. CSI Adaptor and Respective Camera Sensor Module

Two 40-pin Samtec interfaces are provided to support one 4-lane and one 2-lane MIPI CSI-2/D-PHY camera sensor modules on J13 and J14 driving VS680's CSI0 and CSI1 ports respectively. A module-specific adaptor is required along with its respective camera sensor module to be mounted on the interface. Beside MIPI lanes, each interface provides 1.8V, 3.3V, 5.0V and a VIO power supplies, supports I2C and GPIOs to the module&adaptor camera set.

Supported camera sensor:

- OmniVision OV2775 1080p30 image sensor

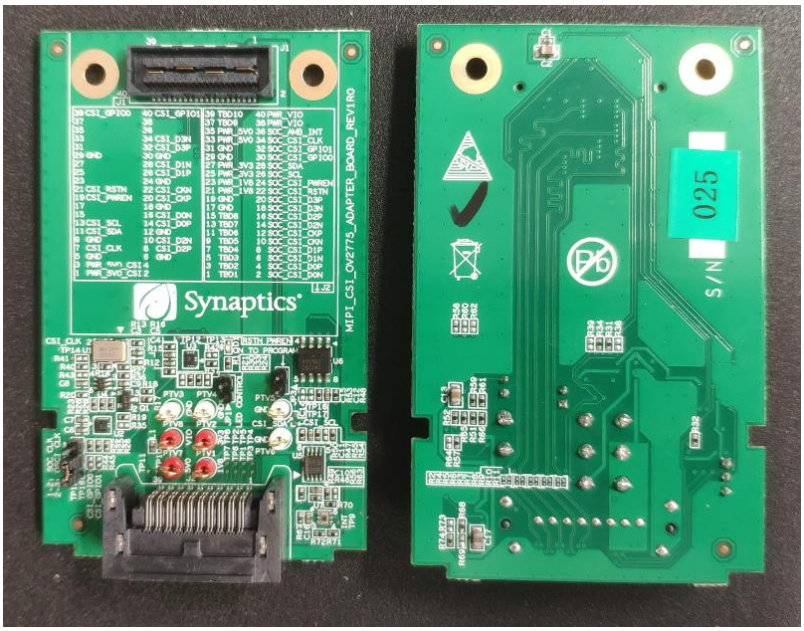


Figure 14. CSI Adaptor for OV2775 Camera Sensor Module (top and bottom views)

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3.3. DSI Adaptor and Respective Display Panel

A 40-pin Samtec interface is provided to support one 4-lane MIPI DSI/D-PHY display panel on J15 driven by VS680's DSI port. A panel-specific adaptor is required along with its respective display panel to be mounted on the interface. Beside MIPI lanes, the interface provides 1.8V, 3.3V, 5.0V, 12V and a VIO power supplies, supports I2C and GPIOs to the panel&adaptor display set. Panel-specific AVDD/AVEE regulators and back light LED drivers are on the adapter board.

Supported display panel:

- Leadtek LTK101P34A002H 10" 1920x1200 landscape panel with LTK10300A0 touch pad

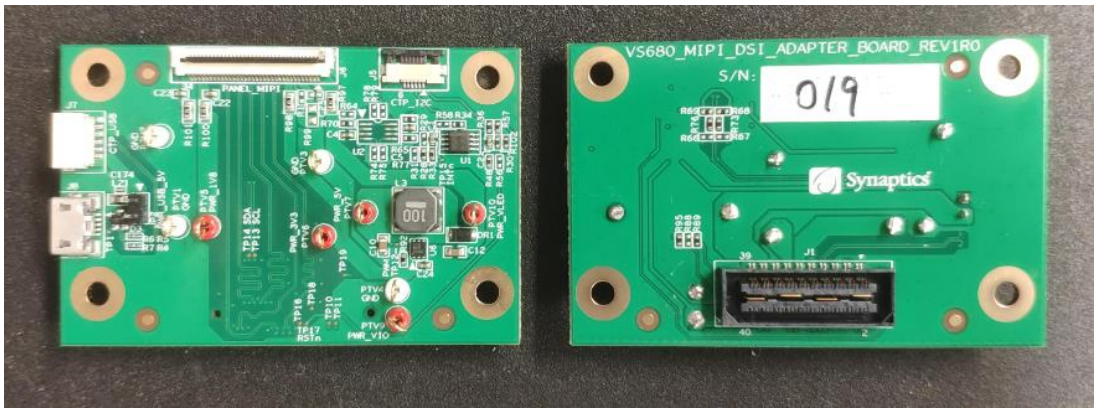


Figure 15. DSI Adaptor for Leadtek 1920x1200 Display Panel (top and bottom views)

3.4. Speaker Card

A dual-row receptacle, J5, is provided for an extension to a multi-channel speaker daughter card from the on-board 15W class-D stereo speaker drivers (CX9000), supporting soundbar with AEC applications. Available cards:

- 2.1-CH Soundbar Speaker Card with 15W class-D (CX9000) and 2W pre-subwoofer (CX22721) drivers
- 7.1-CH Soundbar Speaker Card with 15W class-D (CX9000) and 2W pre-subwoofer (CX22721) drivers

3.5. Soundbar I/O Card

A dual-row receptacle, J9, is provided for an extension card to receive the following audio sources in soundbar:

- a stereo line-in
- a high bit-rate audio bitstream, such as Dolby Atmos or DTS: X, from an HDMI In or eARC of an HDMI Out.
  An eARC receiver on the card outputs audio bitstreams to VS680 over I2S or SPDIF.

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3.6. TSI Card

A dual-row receptacle, J8, is provided for an extension to receive two channels (up four by HW configuration) of RF DTV transport streams. Standards supported:

- DVB T/C/T2
- ISDB T/C

A silicon tuner (Rafael Micro R836H) and demodulator (Sony CXD2856ER) in each channel output DTV content to VS680 over a 4-line STS interface.

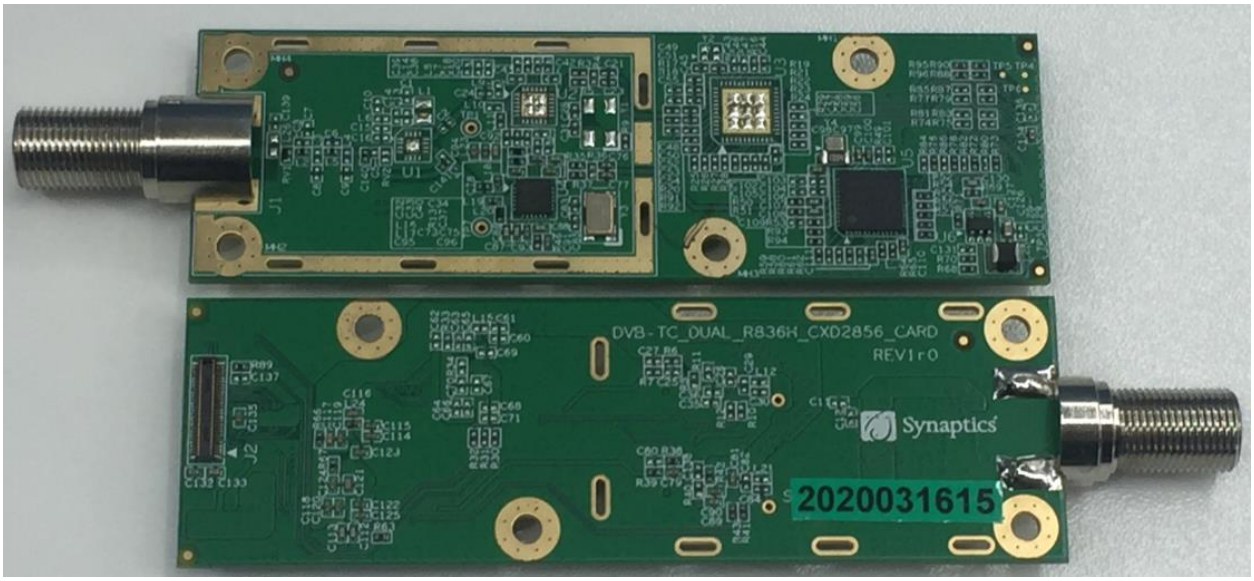


Figure 16. Tuner(R836H) and Demodulator (CXD2856ER) Daughter Card (top and bottom views)

3.7. Fast Ethernet PHY Card

A dual-row receptacle, J27, is provided for the option of supporting a variety of low-cost Fast Ethernet only transceivers.

3.8. M.2 Card

An M.2 E-Key socket, J17, is provided for a variety of modules in the M.2 form factor. Typical applicable modules support WiFi/BT devices with SDIO or PCIE signal interfaces. Available modules:

- Ampak AP12275_M2P with AP6275P 2x2 ac WiFi/BT on M.2 adaptor (Default, PCIe/UART)
- Azurewave AW-CM276MA with 88W8997 2x2 ac WiFi/BT (Option, SDIO/SDIO)
- Azurewave AW-CM358SM with 88W8987 1x1 ac WiFi/BT on M.2 adaptor (Option, SDIO/SDIO)
- Eardatek EWN-8822CSS3AA with RTL8822CS-VS-CG 2x2 ac WiFi/BT on M.2 adaptor (Option, SDIO/UART)

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3.9. Extender M.2 Card

Extender M.2 Card allows up to three cards–one fixed with M.2 edge connector for SDIO signals, plus two each with either M.2 or mini-PCIE edge connector for PCIE signals–to operate simultaneously on the only one M.2 slot that EVK provides. In addition to SDIO/PCIE, all three support USB, UART and I2C signaling.

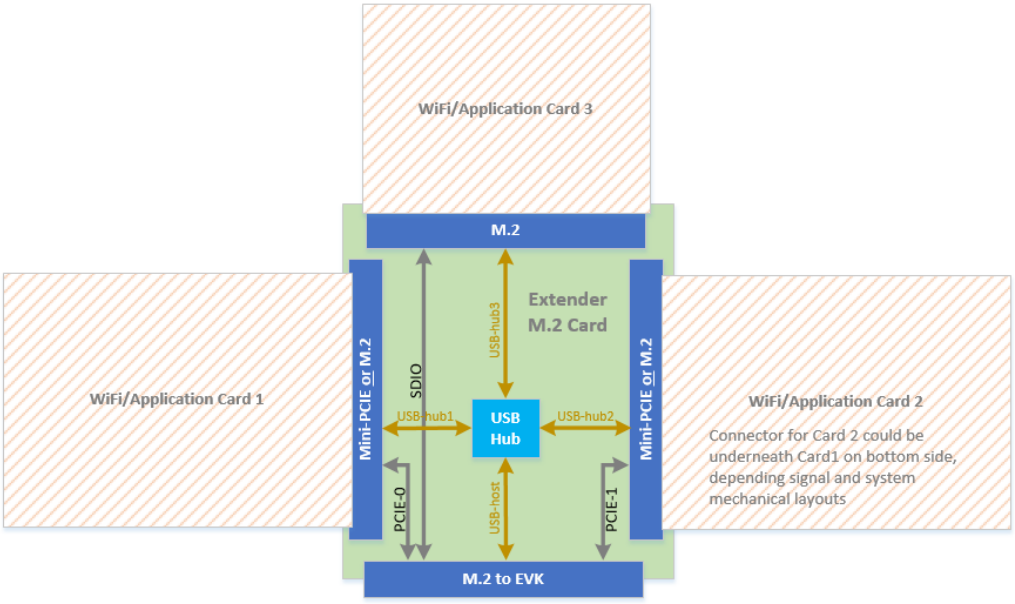


Figure 17. Extender M.2 Physical and Logical Diagram

Table 10 describes connectivity options. The Jumper Short column indicates settings for meeting VIO requirements for specified daughtercards in use on each connector within the extender card.

Note: If the extender card is used, the VIO supplied to the EVK's on-board M.2 connector can remain fixed at a default of 1.8V. Individual VIO settings for each connector within the extender card are selected by using the corresponding jumpers.

Table 10. Extender M.2 Card Connectivity Options and VIO Settings

Option #	Connector Type	Signal Interface	Ref Des	Jumper Short		VIO(V)	Note
Option 1	M.2	SDIO	J2	JP1.2	JP1.1	3.3	Optional
				JP1.2	JP1.3	1.8	Default
	M.2	PCIe0	J4	JP2.2	JP2.1	3.3	Default
				JP2.2	JP2.3	1.8	Optional
	M.2	PCIe1	J5	JP3.2	JP3.1	3.3	Default
				JP3.2	JP3.3	1.8	Optional

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Option 2	M.2	SDIO	J2	JP1.2	JP1.1	3.3	Optional
				JP1.2	JP1.3	1.8	Default
	Mini-PCIe	PCIe0	J3	R102 (0 OHM)		3.3	Fixed
	Mini-PCIe	PCIe1	J6	R124 (0 OHM)		3.3	Fixed
Option 3-1	M.2	SDIO	J2	JP1.2	JP1.1	3.3	Optional
				JP1.2	JP1.3	1.8	Default
	M.2	PCIe0	J4	JP2.2	JP2.1	3.3	Default
				JP2.2	JP2.3	1.8	Optional
	Mini-PCIe	PCIe1	J6	R124 (0 OHM)		3.3	Fixed
Option 3-2	M.2	SDIO	J2	JP1.2	JP1.1	3.3	Optional
				JP1.2	JP1.3	1.8	Default
	Mini-PCIe	PCIe0	J3	R102 (0 OHM)		3.3	Fixed
	M.2	PCIe1	J5	JP3.2	JP3.1	3.3	Default
				JP3.2	JP3.3	1.8	Optional

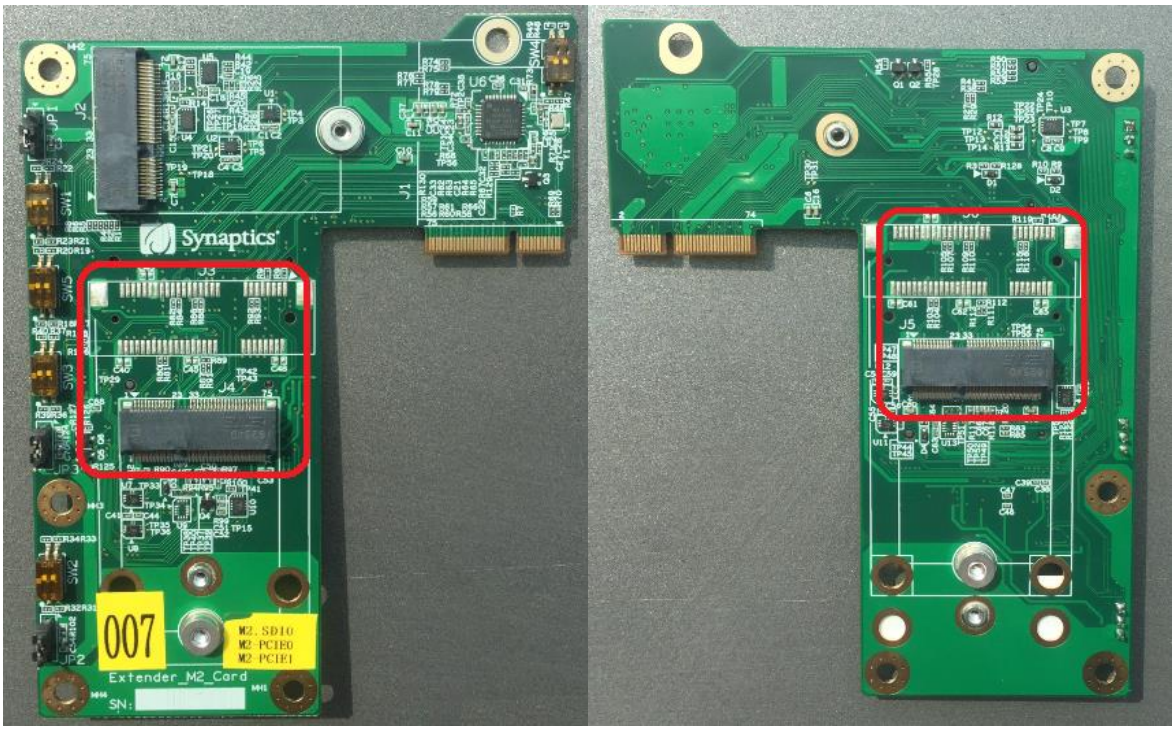


Figure 18. Extender M.2 Card with Option1 (top and bottom views)

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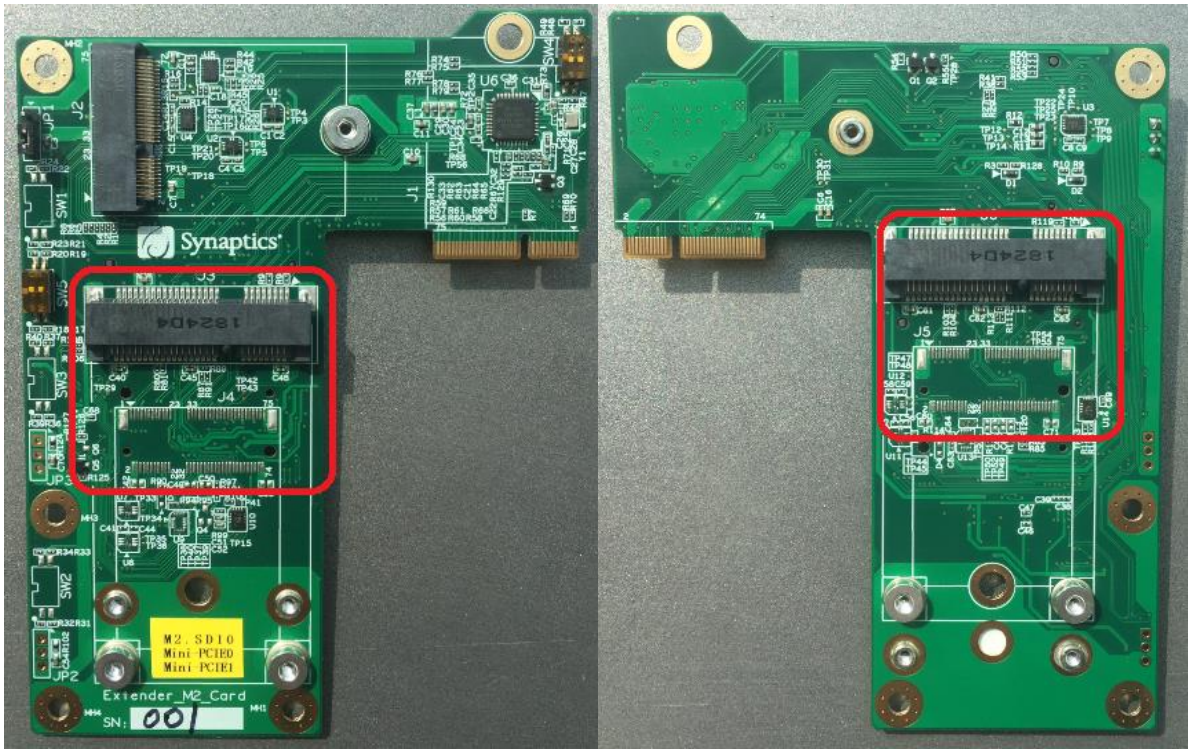


Figure 19. Extender M.2 Card with Option2 (top and bottom views)

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3.10. DMIC Card

A digital MEMS Microphone (DMIC) card can be mounted on MIC interface J10 to provide up to 4 channels of PDM signal to VS680. Available DMIC cards using Infineon IM69D130V01 mic:

Table 11. DMIC Cards

Synaptics P/N	# of MIC	MIC Separation	Form Factor	Mute/LED Modes
GVA_MIC-DC_REV1R1	2	69mm	Linear	AVS, GVA
950-C00928	2	55mm	Linear	AVS
950-C00926	2	Variable	Linear	AVS
950-C00987	4	Variable	Linear	AVS, GVA
950-C00921	4	Variable	Round	AVS

GVA_MIC-DC_REV1R1 and 950-C00928 are the two most commonly used.

3.10.1. GVA_MIC-DC_REV1R1 DMIC

GVA_MIC-DC_REV1R1 features two mute and LED modes:

- AVS (JP1=1-2, both sliding switches in SW4=ON)
  - SW3 momentary push-button to VS680 GPIO input to request mute/unmute
  - VS680 responds to the mute/unmute request by sending a GPIO output to turn-off/on power to DMIC, its signal path, and turn-on/off Mute LED D1, respectively
  - LED D2 flashes once when the trigger word is detected
- GVA (JP1=2-3, both sliding switches in SW4=OFF)
  - Sliding SW2 to 1/3 positions to turn-on/off power to DMIC, its signal path respectively, this state is read by VS680 GPIO input
  - I2C controls 4 multi-color LEDs

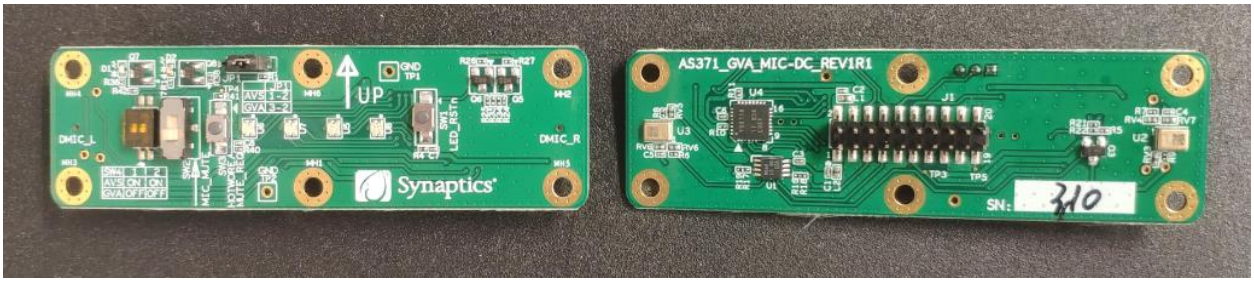


Figure 20. GVA_MIC-DC_REV1R1 Fixed-2 DMIC Card (top and bottom view)

3.10.2. 950-C00928 DMIC

950-C00928 features:

- Momentary push-button SW1 to VS680 GPIO input to request mute/unmute
- VS680 responds to the mute/unmute request by sending a GPIO output to turn-off/on power to DMIC, its signal path, and turn-on/off Mute LED D25, respectively
- LED D26 flashes once when the trigger word is detected.

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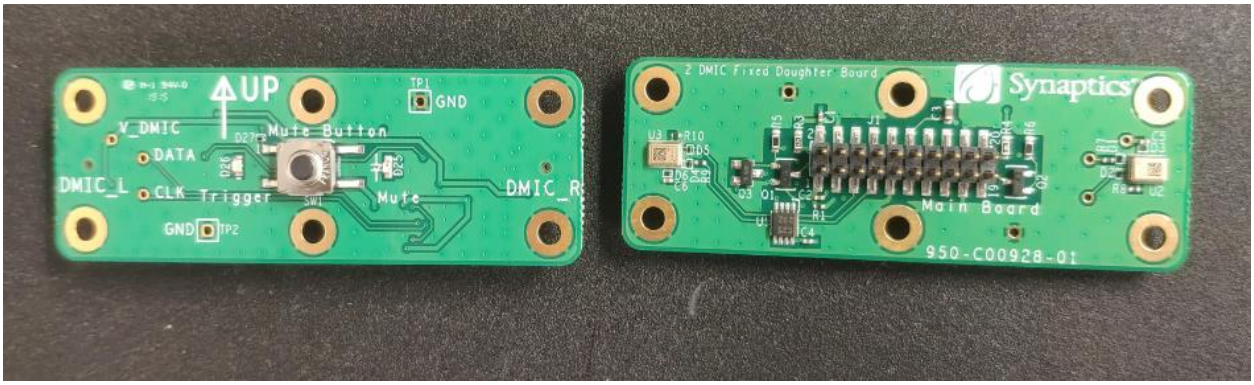


Figure 21. 950-C00928 Fixed-2 DMIC Card (top and bottom view)

3.10.3. Other DMIC Cards

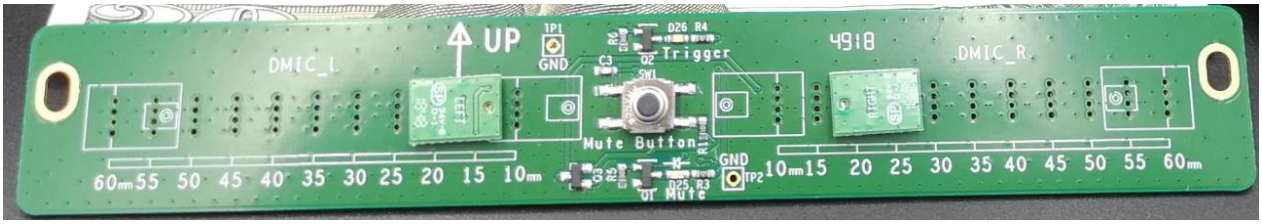


Figure 22. 950-C00926 Variable-2 DMIC

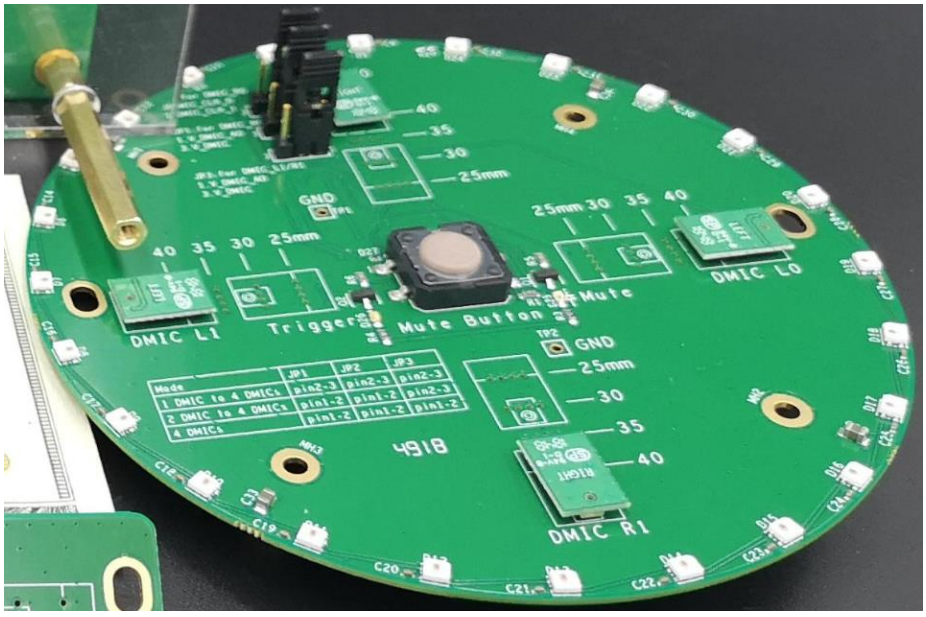


Figure 23. 950-C00921 Variable-4 DMIC

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3.11. Pin-demuxing for Standard Interface Configuration

This section covers pin-demuxing configuration for VS680 EVK applications. For System Manager (SM), listed in Table 12. For System on Chip (SoC), please refer to Table 13.

Table 12. SM Pin-demuxing Usage

VS680 System Manager (SM) Domain				
Pad/Pin Name		**Default Usage**	**Direction**	**Mode Setting**
SM_TWSI	SM_TW2_SCL	IO:RX_EDID_SCL	OUT	MODE_0
	SM_TW2_SDA	IO:RX_EDID_SDA	IN/OUT	MODE_0
	SM_TW3_SCL	IO:SM_TW3_SCL	OUT	MODE_1
	SM_TW3_SDA	IO:SM_TW3_SDA	IN/OUT	MODE_1
SM_JTAG	SM_TMS	IO:SM_GPIO[6]	OUT	MODE_1
	SM_TDI	IO:SM_GPIO[7]	IN	MODE_1
	SM_TDO	IO:SM_GPO[8]	OUT	MODE_1
SM_UART0/1	SM_URT0_TXD	O:SM_URT0_TXD	OUT	MODE_0
	SM_URT0_RXD	I:SM_URT0_RXD	IN	MODE_0
	SM_URT1_TXD	IO:SM_TW2B_SCL	OUT	MODE_6
	SM_URT1_RXD	IO:SM_TW2B_SDA	IN/OUT	MODE_6
SM_SPI2	SM_SPI2_SS0n	IO:SM_GPO[17]	OUT	MODE_1
	SM_SPI2_SS1n	IO:SM_GPO[16]	OUT	MODE_0
	SM_SPI2_SS2n	O:URT2_TXD	OUT	MODE_5
	SM_SPI2_SS3n	I:URT2_RXD	IN	MODE_5
	SM_SPI2_SDO	O:URT2_RTSn	OUT	MODE_2
	SM_SPI2_SDI	I:URT2_CTSn	IN	MODE_2
	SM_SPI2_SCLK	IO:SM_GPIO[11]	IN	MODE_1
SM_HDMI	SM_HDMI_TX_HPD	IO:SM_GPIO[2]	IN/OUT	MODE_0
	SM_HDMI_CEC	IO:SM_HDMI_CEC	IN	MODE_1
	SM_HDMI_RX_HPD	IO:SM_GPIO[20]	IN	MODE_1
	SM_HDMI_RX_PWR5V	I:SM_HDMIRX_PWR5V	IN	MODE_0

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Table 13. SoC Pin-demuxing Usage

VS680 System-on-chip (SoC) Domain				
Pad/Pin Name		**Default Usage**	**Direction**	**Mode Setting**
SDIO	SDIO_CDn	IO:SDIO_CDn	IN	MODE_0
	SDIO_WP	IO:GPIO[44]	IN	MODE_1
SPI1	SPI1_SS0n	O:SPI1_SS0n	OUT	MODE_0
	SPI1_SS1n	O:PWM[1]	OUT	MODE_4
	SPI1_SS2n	IO:TW1B_SCL	OUT	MODE_3
	SPI1_SS3n	IO:TW1B_SDA	IN/OUT	MODE_3
	SPI1_SDO	O:SPI1_SDO	OUT	MODE_0
	SPI1_SCLK	O:SPI1_SCLK	OUT	MODE_0
	SPI1_SDI	I:SPI1_SDI	IN	MODE_0
TW0	TW0_SCL	IO:TW0_SCL	OUT	MODE_1
	TW0_SDA	IO:TW0_SDA	IN/OUT	MODE_1
STS0/1	STS0_CLK	I:STS0_CLK	IN	MODE_1
	STS0_SOP	I:STS0_SOP	IN	MODE_1
	STS0_SD	I:STS0_SD	IN	MODE_1
	STS0_VALD	I:STS0_VALD	IN	MODE_1
	STS1_CLK	I:STS1_CLK	IN	MODE_1
	STS1_SOP	I:STS1_SOP	IN	MODE_1
	STS1_SD	I:STS1_SD	IN	MODE_1
	STS1_VALD	I:STS1_VALD	IN	MODE_1
USB2	USB2_DRV_VBUS	IO:GPIO[55]	IN	MODE_1
RGMII	RGMII_MDC	O:RGMII_MDC	OUT	MODE_0
	RGMII_MDIO	IO:RGMII_MDIO	IN/OUT	MODE_0
	RGMII_TXC	O:RGMII_TXC	OUT	MODE_0
	RGMII_TXD[0]	O:RGMII_TXD[0]	OUT	MODE_0
	RGMII_TXD[1]	O:RGMII_TXD[1]	OUT	MODE_0
	RGMII_TXD[2]	O:RGMII_TXD[2]	OUT	MODE_0
	RGMII_TXD[3]	O:RGMII_TXD[3]	OUT	MODE_0
	RGMII_TXCTL	O:RGMII_TXCTL	OUT	MODE_0
	RGMII_RXC	I:RGMII_RXC	IN	MODE_0
	RGMII_RXD[0]	I:RGMII_RXD[0]	IN	MODE_0
	RGMII_RXD[1]	I:RGMII_RXD[1]	IN	MODE_0

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VS680 System-on-chip (SoC) Domain				
Pad/Pin Name		**Default Usage**	**Direction**	**Mode Setting**
	RGMII_RXD[2]	I:RGMII_RXD[2]	IN	MODE_0
	RGMII_RXD[3]	I:RGMII_RXD[3]	IN	MODE_0
	RGMII_RXCTL	I:RGMII_RXCTL	IN	MODE_0
I2S1	I2S1_DO[0]	O:I2S1_DO[0]	OUT	MODE_1
	I2S1_DO[1]	O:I2S1_DO[1]	OUT	MODE_1
	I2S1_DO[2]	O:I2S1_DO[2]	OUT	MODE_1
	I2S1_DO[3]	O:I2S1_DO[3]	OUT	MODE_1
	I2S1_LRCK	IO:I2S1_LRCKIO	IN/OUT	MODE_1
	I2S1_BCLK	IO:I2S1_BCLKIO	IN/OUT	MODE_1
	I2S1_MCLK	IO:I2S1_MCLK	OUT	MODE_1
SPDIF	SPDIFO	O:SPDIFO	IN	MODE_1
	SPDIFI	I:PDMC_DI	IN	MODE_2
I2S2	I2S2_LRCK	IO:I2S2_LRCKIO	IN/OUT	MODE_1
	I2S2_BCLK	IO:I2S2_BCLKIO	IN/OUT	MODE_1
	I2S2_DI[0]	I:I2S2_DI[0]	IN	MODE_1
	I2S2_DI[1]	I:I2S2_DI[1]	IN	MODE_1
	I2S2_DI[2]	I:I2S2_DI[2]	IN	MODE_1
	I2S2_DI[3]	I:I2S2_DI[3]	IN	MODE_1
	I2S2_MCLK	IO:PDMB_CLKIO	IN/OUT	MODE_2
HDMI_TX_EDDC	HDMI_TX_EDDC_SCL	IO:TX_EDDC_SCL	IN	MODE_0
	HDMI_TX_EDDC_SDA	IO:TX_EDDC_SDA	IN/OUT	MODE_0
I2S3	I2S3_DO	O:I2S3_DO	OUT	MODE_1
	I2S3_LRCK	IO:I2S3_LRCKIO	IN/OUT	MODE_1
	I2S3_BCLK	IO:I2S3_BCLKIO	IN/OUT	MODE_1
	I2S3_DI	I:I2S3_DI	IN	MODE_1

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3.12. Pin-demuxing for GPIO/GPO Configuration

This section covers pin-demuxed GPIO/GPO usage of SM & SOC domains.

Table 14. SM GPIO/GPO Usage

VS680 SM GPIO/GPO	Availability	Direction	Default Function	GPIO Signaling
SM_GPIO [0]	Not Available	OUT	IO:RX_EDID_SCL	—
SM_GPIO [1]	Not Available	IN/OUT	IO:RX_EDID_SDA	—
SM_GPIO [2]	MODE_0	IN	IR	Input for IR Receiver;
SM_GPIO [3]	Not Available	OUT	SM_HDMI_CEC	—
SM_GPIO [4]	Not Available	OUT	IO:SM_TW2B_SCL	—
SM_GPIO [5]	Not Available	IN/OUT	IO:SM_TW2B_SDA	—
SM_GPIO [6]	MODE_1	IN	M2-W_WAKE#	0: Triggered 1: Idle;
SM_GPIO [7]	MODE_1	IN	GePHY_WAKE#	0: Triggered 1: Idle;
SM_GPIO [8]	MODE_1	OUT	DMIC_TRIG_LED	0: Idle 1: LED triggered;
SM_GPIO [9]	MODE_0	OUT	IO:SM_TW3_SCL	—
SM_GPIO [10]	MODE 0	IN/OUT	IO:SM_TW3_SDA	—
SM_GPIO [11]	MODE 1	IN	DMIC_MUTE_REQ	0: Idle 1: Triggered;
SM_GPIO [12]	MODE 1	IN	I:URT2_CTSn	—
SM_GPIO [13]	MODE 1	OUT	O:URT2_RTSn	—
SM_GPIO [14]	MODE 1	OUT	I:URT2_RXD	—
SM_GPIO [15]	MODE 1	OUT	O:URT2_TXD	—
SM_GPIO [16]	MODE 0	OUT	HDMI-TX_PWR_ON	0: Disabled 1: Enabled;
SM_GPIO [17]	MODE 1	OUT	Not Assigned	Idle
SM_GPIO [18]	Not Available	OUT	I:SM_URT0_RXD	—
SM_GPIO [19]	Not Available	OUT	O:SM_URT0_TXD	—
SM_GPIO [20]	MODE 1	IN	SM_GPIO-EXPD_INT-REQ#	0: Triggered 1: Idle;
SM_GPIO [21]	Not Available	IN	I:SM_HDMIRX_PWR5V	—

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Table 15. SoC GPIO/GPO Usage

VS680 SoC GPIO/GPO	Availability	Direction	Default Function	GPIO Signaling
SOC_GPIO[0]	Not Available	IN	I:I2S3_DI	—
SOC_GPIO[1]	Not Available	OUT	O:I2S3_DO	—
SOC_GPIO[2]	Not Available	IN/OUT	IO:I2S3_BCLKIO	—
SOC_GPIO[3]	Not Available	OUT	IO:I2S3_LRCKIO	—
SOC_GPIO[4]	Not Available	IN	I:PDMC_DI	—
SOC_GPIO[5]	Not Available	IN/OUT	IO:TX_EDDC_SDA	—
SOC_GPIO[6]	Not Available	OUT	IO:TX_EDDC_SCL	—
SOC_GPIO[7]	Not Available	OUT	IO:PDMB_CLKIO	—
SOC_GPO[8]	Not Available	IN	I:I2S2_DI[3]	—
SOC_GPO[9]	Not Available	IN	I:I2S2_DI[2]	—
SOC_GPO[10]	Not Available	IN	I:I2S2_DI[1]	—
SOC_GPO[11]	Not Available	IN	I:I2S2_DI[0]	—
SOC_GPO[12]	Not Available	IN/OUT	IO:I2S2_BCLKIO	—
SOC_GPO[13]	Not Available	IN/OUT	IO:I2S2_LRCKIO	—
SOC_GPO[14]	Not Available	OUT	O:SPDIFO	—
SOC_GPO[15]	Not Available	OUT	O:I2S1_DO[3]	—
SOC_GPO[16]	Not Available	OUT	O:I2S1_DO[2]	—
SOC_GPIO[17]	Not Available	OUT	O:I2S1_DO[1]	—
SOC_GPIO[18]	Not Available	OUT	IO:I2S1_MCLK	—
SOC_GPIO[19]	Not Available	OUT	O:I2S1_DO[0]	—
SOC_GPIO[20]	Not Available	IN/OUT	IO:I2S1_BCLKIO	—
SOC_GPIO[21]	Not Available	IN/OUT	IO:I2S1_LRCKIO	—
SOC_GPIO[22]	Not Available	OUT	O:RGMII_TXCTL	—
SOC_GPIO[23]	Not Available	OUT	O:RGMII_TXC	—
SOC_GPIO[24]	Not Available	OUT	O:RGMII_TXD[3]	—
SOC_GPIO[25]	Not Available	OUT	O:RGMII_TXD[2]	—
SOC_GPIO[26]	Not Available	OUT	O:RGMII_TXD[1]	—
SOC_GPIO[27]	Not Available	OUT	O:RGMII_TXD[0]	—
SOC_GPIO[28]	Not Available	IN/OUT	IO:RGMII_MDIO	—
SOC_GPIO[29]	Not Available	OUT	O:RGMII_MDC	—
SOC_GPIO[30]	Not Available	IN	I:RGMII_RXCTL	—

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VS680 SoC GPIO/GPO	Availability	Direction	Default Function	GPIO Signaling
SOC_GPIO[31]	Not Available	IN	I:RGMII_RXC	—
SOC_GPIO[32]	Not Available	IN	I:RGMII_RXD[3]	—
SOC_GPIO[33]	Not Available	IN	I:RGMII_RXD[2]	—
SOC_GPIO[34]	Not Available	IN	I:RGMII_RXD[1]	—
SOC_GPIO[35]	Not Available	IN	I:RGMII_RXD[0]	—
SOC_GPIO[36]	Not Available	IN	I:STS1_VALD	—
SOC_GPIO[37]	Not Available	IN	I:STS1_SD	—
SOC_GPIO[38]	Not Available	IN	I:STS1_SOP	—
SOC_GPIO[39]	Not Available	IN	I:STS1_CLK	—
SOC_GPIO[40]	Not Available	IN	I:STS0_VALD	—
SOC_GPIO[41]	Not Available	IN	I:STS0_SD	—
SOC_GPIO[42]	Not Available	IN	I:STS0_SOP	—
SOC_GPIO[43]	Not Available	IN	I:STS0_CLK	—
SOC_GPIO[44]	MODE_1	IN	SPK_INT_REQ	0: Idle 1: Triggered;
SOC_GPIO[45]	Not Available	IN	IO:SDIO_CDn	—
SOC_GPIO[46]	Not Available	IN	IO:TW0_SDA	—
SOC_GPO[47]	Not Available	OUT	IO:TW0_SCL	—
SOC_GPO[48]	Not Available	OUT	IO:TW0_SCL	—
SOC_GPO[49]	Not Available	OUT	IO:TW0_SCL	—
SOC_GPO[50]	Not Available	OUT	IO:TW0_SCL	—
SOC_GPO[51]	Not Available	OUT	IO:TW0_SCL	—
SOC_GPO[52]	Not Available	OUT	IO:TW0_SCL	—
SOC_GPO[53]	Not Available	OUT	IO:TW0_SCL	—
SOC_GPO[54]	Not Available	OUT	IO:TW0_SCL	—
SOC_GPO[55]	MODE_1	IN	SOC_GPIO-EXPD_INT-REQ#	0: Triggered 1: Idle;

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3.13. GPIO Expanders Over I2C

Due to the large number of functionality covered by VS680 EVK, most VS680 digital pins that have GPIO/GPO pin-demux option have been used for other functions. As such, GPIO expanders are used extensively to supplement system control purposes.

Table 16. GPIO Expanders Usage

Expander GPIO/GPO	I2C#	Domain	Voltage	Direction	Function	GPIO Signaling
GPIO0_0	SM_TW3	SM	1.8V	OUT	VCORE_ON#	0: Assertion 1: De-assertion
GPIO0_1	SM_TW3	SM	1.8V	OUT	VCPU_ON#	0: Assertion 1: De-assertion
GPIO0_2	SM_TW3	SM	1.8V	OUT	VDDM_ON#	0: Assertion 1: De-assertion
GPIO0_3	SM_TW3	SM	1.8V	OUT	VDDM-LPQ_OFF	0: De-assertion 1: Assertion
GPIO0_4	SM_TW3	SM	1.8V	OUT	STAND-BY_EN	0: De-assertion 1: Assertion
GPIO0_5	SM_TW3	SM	1.8V	OUT	DMIC-MUTE_EN& BHF_EN	0: Unmute DMIC & Disable BHF 1: Mute DMIC & Enable BHF
GPIO0_6	SM_TW3	SM	1.8V	IN	M2-PCIe_CLKREQ#	0: Triggered 1: Idle
GPIO0_7	SM_TW3	SM	1.8V	IN	M2-PCIe_WAKE#	0: Triggered 1: Idle
GPIO1_0	SM_TW3	SM	3.3V	OUT	GePHY_RST#	0: Assertion 1: De-assertion
GPIO1_1	SM_TW3	SM	3.3V	OUT	M2-PCIe_RST#	0: Assertion 1: De-assertion
GPIO1_2	SM_TW3	SM	3.3V	OUT	M2-W_DISABLE1#	0: Assertion 1: De-assertion
GPIO1_3	SM_TW3	SM	3.3V	OUT	M2-W_HOST-WAKE#	0: Assertion 1: De-assertion
GPIO1_4	SM_TW3	SM	3.3V	OUT	HDMI-RX_HPD_MUTEn	0: Forced to LOW 1: Aligned with HDMI5V
GPIO1_5	SM_TW3	SM	3.3V	OUT	M2-W_DISABLE2#	0: Assertion 1: De-assertion
GPIO1_6	SM_TW3	SM	3.3V	IN/OUT	MIPI-CSI1_GPIOA	RSVD for MIPI-CSI1 CTRL
GPIO1_7	SM_TW3	SM	3.3V	IN/OUT	MIPI-CSI1_GPIOC	RSVD for MIPI-CSI1 CTRL
GPIO2_0	SOC_TW0	SOC	3.3V	OUT	SOC_GLOBAL_RSTn	0: Assertion 1: De-assertion

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Expander GPIO/GPO	I2C#	Domain	Voltage	Direction	Function	GPIO Signaling
GPIO2_1	SOC_TWO	SOC	3.3V	IN	USB3-SLOT_OCn	0: Assertion 1: De-assertion
GPIO2_2	SOC_TWO	SOC	3.3V	OUT	USB3-SLOT_PWR_ON	0: De-assertion 1: Assertion
GPIO2_3	SOC_TWO	SOC	3.3V	OUT	USB2-SLOT_PWR_ON	0: De-assertion 1: Assertion
GPIO2_4	SOC_TWO	SOC	3.3V	OUT	PDM_DATA_SEL	0: SPDIFIN 1: I2S2_DAT
GPIO2_5	SOC_TWO	SOC	3.3V	OUT	MIPI-CSI0_GPIOB	RSVD for MIPI-CSI0 CTRL
GPIO2_6	SOC_TWO	SOC	3.3V	OUT	MIPI-CSI0_GPIOA	RSVD for MIPI-CSI0 CTRL
GPIO2_7	SOC_TWO	SOC	3.3V	OUT	MIPI-CSI0_GPIOC	RSVD for MIPI-CSI0 CTRL
GPIO3_0	SOC_TWO	SOC	3.3V	IN	USB2-SLOT_OCn	0: Assertion 1: De-assertion
GPIO3_1	SOC_TWO	SOC	3.3V	OUT	MicroSD-SLOT_PWR_ON	0: De-assertion 1: assertion
GPIO3_2	SOC_TWO	SOC	3.3V	OUT	MIPI-DSI_BLON	0: De-assertion 1: assertion
GPIO3_3	SOC_TWO	SOC	3.3V	OUT	MIPI-DSI_TE	0: De-assertion 1: assertion
GPIO3_4	SOC_TWO	SOC	3.3V	IN	MIPI-DSI_TPINTn	0: Triggered 1: Idle
GPIO3_5	SOC_TWO	SOC	3.3V	OUT	MIPI-DSI_RESETn	0: Assertion 1: De-assertion
GPIO3_6	SOC_TWO	SOC	3.3V	OUT	SOC-2S2_SRC_SEL	0: From eARC-RX 1: From 2CH ADC
GPIO3_7	SOC_TWO	SOC	3.3V	OUT	SOC_ SPDIF-IN_SRC_SEL	0: From TosLink-RX 1: From eARC-RX

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3.14. I2C Bus

Table 17 describes EVK's usage of I²C bus, the equivalence of VS680's Two Wire Serial Interface (TWSI) bus.

Table 17. I2C Bus Descriptions

I²C/TWSI Bus	Device	Part Number	Ref Des	Slave Address (7-bit)	Location
SM_TW3	IC GPIO EXPANDER I2C 8Bit	FXL6408UMX	U12	0x43	Main-Board
	IC GPIO EXPANDER I2C 8Bit	FXL6408UMX	U13	0x44	Main-Board
	IC RTC CLK/CALENDAR	DS1339AU+T	U63	0x68	Main-Board
	IC Translating Switch Interface	PCA9543APWR	U50	0x70	Main-Board
SM_TW2B	IC REG, 0.8V Vout ,12.5mV Step 6A, 0.600V to 1.3875V Vout, Fsw 2.4MHz, Step-Down Convertor with I2C, CSP-20, Silergy	SY8827NPKC	U65	0x60	Main-Board
	IC REG,4.5V to 17V Vin, 0.6V to 1.87V Vout, 10mV Steps, 8A, default 0.5MHz synchronous Step-Down Convertor through I2C interface, QFN-14, MPS	MP8867GLE	U41	0x62	Main-Board
SOC_TW1B	IC REG, 0.8V Vout ,12.5mV Step 6A, 0.600V to 1.3875V Vout, Fsw 2.4MHz, Step-Down Convertor with I2C, CSP-20, Silergy	SY8827NPKC	U66	0x60	Main-Board
	IC REG,4.5V to 21V Vin, 0.6V to 1.87V Vout, 10mV Steps, 4A, default 0.6MHz synchronous Step-Down Convertor through I2C interface, QFN-15, MPS	MP8864GQ	U40	0x68	Main-Board
SOC_TW0	IC,High Power Stereo Class D Amplifier with Advanced Speaker	CX9000-11Z	U20	0x33	Main-Board
	IC GPIO EXPANDER I2C 8Bit	FXL6408UMX	U14	0x43	Main-Board
	IC GPIO EXPANDER I2C 8Bit	FXL6408UMX	U15	0x44	Main-Board
TX_EDDC	EDDC Bus for HDMI TX	HDMI Source	J12	0x3A/0x50	Main-Board
RX_EDDC	EDDC Bus for HDMI RX	HDMI Sink	J11	0x3A/0x50	Main-Board

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4. Bringing Up the VS680 EVK System

4.1. Connecting External Components and Performing Hardware Testing

Do the following to connect external components to VS680 EVK Main Board:

6. Connect an AC-DC 12V power supply to J24. Do not power up VS680 EVK Main Board until making all connections listed in this section and Hardware Jumper Settings in Table 5 are done;
7. Connect SPI Card to J1, Debug Board to J23 and TV to HDMI Out J12 with a HDMI cable;
8. Insert USB3.0/2.0 flash disc to J21/J20 over adaptor and external loop-back cable to J2;
9. Insert M.2 adaptor to J17 with both M.2 SDIO and PCIe devices stuffed.

If no short issues, power up the system and check voltages as shown in Table 18 with the LED status shown in Table 1. Once these items are checked to satisfactory, proceed to steps described in Software Testing.

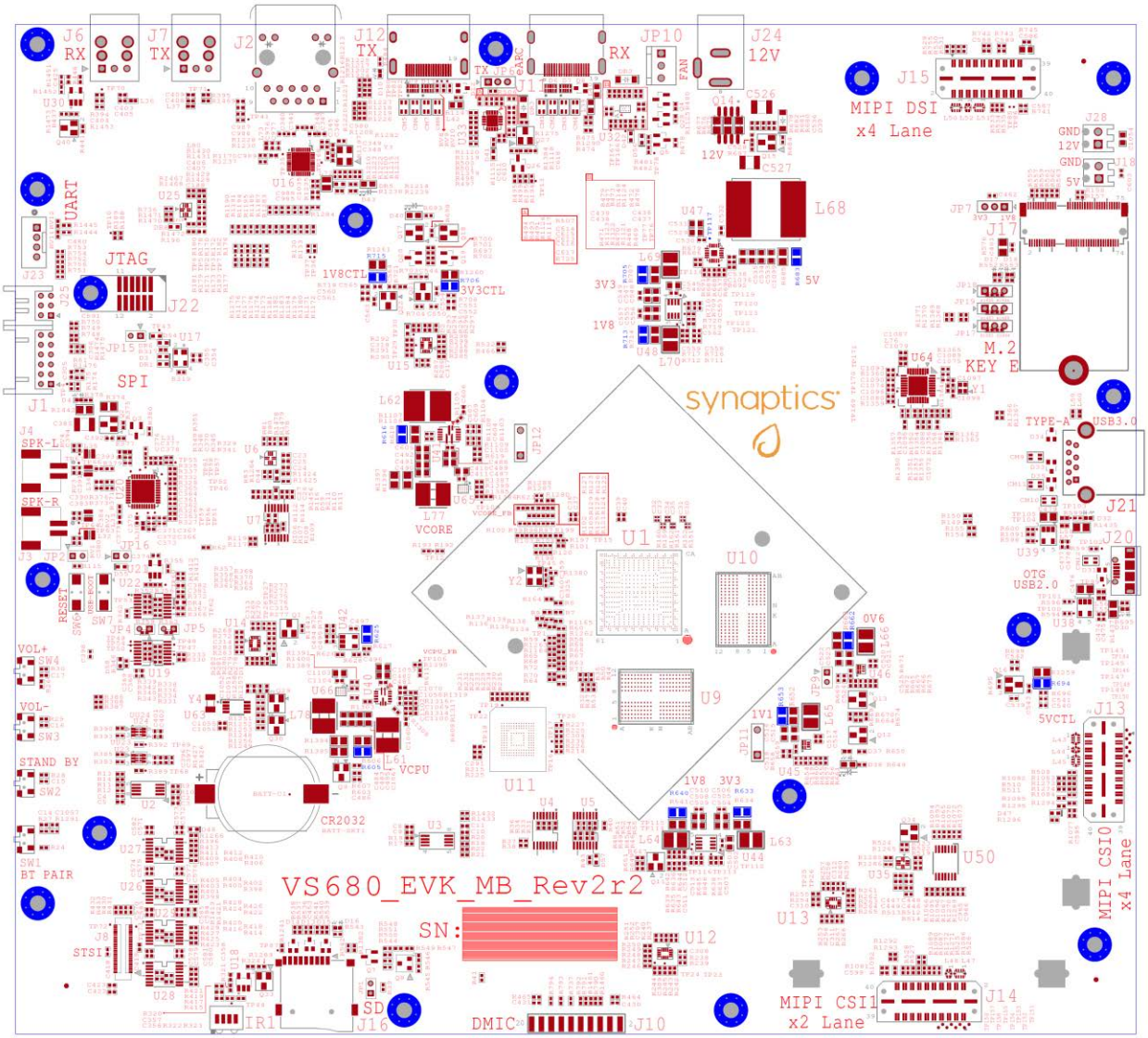


Figure 24. Short and voltage check points

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Table 18 Short and Voltage Check Points using any Test Point for Ground

Ref Des	Form	Signal	Voltage
TP117	SMD pad	PWR_12V	12V +/- 2% [11.76,12.24]
R683	Either pad	PWR_5V	5V +/- 2% [4.90,5.10]
R694	Either pad	PWR_5V_CTL	5V +/- 2% [4.90,5.10]
R705	Either pad	PWR_3V3	3.3V +/- 1% [3.267,3.333]
R706	Either pad	PWR_3V3_CTL	3.3V +/- 1% [3.267,3.333]
R713	Either pad	PWR_1V8	1.8V +/- 2% [1.764,1.836]
R715	Either pad	PWR_1V8_CTL	1.8V +/- 2% [1.764,1.836]
R633	Either pad	PWR_3V3-M2	3.3V +/- 1% [3.267,3.333]
R640	Either pad	PWR_VDDM_1V8	1.8V +/- 2% [1.764,1.836]
R653	Either pad	PWR_VDDM_1V1	1.1V +/- 2% [1.078,1.122]
R662	Either pad	PWR_VDDM_1V1&0V6	0.6V +/- 2% [0.588,0.612]
R616	Either pad	PWR_SoC_VCORE	0.8V +/- 2% [0.784,0.816]
R605	Either pad	PWR_SoC_VCPU	0.8V +/- 2% [0.784,0.816]
R625	Either pad	PWR_VDD_SM	0.8V +/- 2% [0.784,0.816]]
MH1 to MH18	Hole pad	GND	—

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4.2. Software Testing

4.2.1. Diagnostics

The following scripts are used to bring up the system.

1. Mandatory script: bg7_all_xxx.ttl. This script covers the majority of hardware interfaces: DDR, CPU, NNA, GFX3D, V4G Decoder, VPP, H1, SM, HDMI TX, eMMC chip, RGMII, TWSI_0/1/2/3, SDIO-IO, PCIe, USB3.0/2.0 host tests. Please make sure that jumper at JP1 and M2 adaptor are stuffed.
2. Optional 1 script: BG7_xxx_SPDIF_LPBK.ttl: This script covers SPDIF loop back from TX to RX over external cable connection.
3. Optional 2 script: BG7_xxx_ I2S_2CH_48K_CX9000.ttl: This script covers I2S1 to on-board 2CH speaker IC CX9000 with audio playing back over stereo speakers.
4. Optional 3 script: bg7_sdio-mem_xxx.ttl.ttl. This script covers SDIO memory card test. Before it's running, please check if Micro SD card is inserted at J16 and 2pin 2.0mm pitch Jumper at JP1 is removed.
5. Optional 4 script: BG7_3min_stress_xxx.ttl. This script covers SOC stability test with heavy stresses, mainly for SOC internal IPs like CPU/DDR/GPU/V4G.

4.2.2. Software Application Testing

TBD

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5. References

The following documents are applicable to the VS680 EVK, Revision 2.2 release:

- TBD

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6. Revision History

Last Modified	Revision	Description
February 2020	1	Preliminary release.
August 2023	2	

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